Final Technical Report

SiC Discrete Power Devices

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First Order Analysis of Unipolar Versus Bipolar SiC Devices - Vertical Channel UMESFET - A Planar Lateral Channel SiC Vertical High Power JFET-The Planar Lateral Channel MESFET-Analysis & Optimization of the Planar 6H-SiC ACCUFET-Comparison of 6H-SiC & 4H-SiC High Voltage Planar ACCUFETs-Design & Development of Process Routes Leading to 4" dia.SiC.

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13. ABSTRACT (*Maxim*

A first order analysis, to determine the voltage-ratings up to which unipolar devices have lower forward voltage drop than bipolar devices, is performed. Further, problems associated with the operation of a SiC MOSFET and alternatives to the MOSFET are considered. The performance of a 1000 V 4H-SiC U-MESFET was studied using numerical simulations and the results are presented. Problems associated in fabricating the U-MESFET structure are discussed. In addition, a novel trench-gate heterojunction FET (HJFET) structure is analyzed.

In addition, a novel planar lateral channel SiC high power JFET is described. A novel planar lateral channel SiC MESFET structure with vertical current flow in the drift region is also proposed and demonstrated by modeling and fabrication. Further, a novel planar accumulation channel SiC MOSFET structure called ACCUFET is reported. The problems of gate oxide rupture and poor channel conductance previously reported in SiC UMOSFETs are solved by using a buried P+ layer to shield the channel region. The fabricated 6H-SiC unterminated devices had a blocking voltage of 350 V with a specific on-resistance of 18 mΩ-cm^2 at room temperature for a gate bias of only 5 V. A comparison of 6H-SiC and 4H-SiC high voltage planar ACCUFETs is presented. Finally, the design and development of process routes leading to 4" diameter SiC substrates are described.

14. SUBJECT TERMS
Silicon Carbide, ACCUFET, MOSFET, JFET, MESFET, Breakdown Voltage, Specific On-Resistance, Chemical Vapor Deposition, RHEED

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I. Introduction

At present, semiconductor power devices are commonly used to control heavy machinery and equipment. The principal semiconductor from which these power devices are manufactured is silicon. For many applications, the power MOSFET is the commonly used device. In order to minimize the power losses in the power MOSFET, it is necessary to reduce the on-resistance of the device. Progress in silicon power technology has been successful in pushing the on-resistance of the MOSFET close to the theoretical limits [1,2]. It is therefore necessary to consider other semiconductor materials if further improvements in device performance need to be attained. Silicon Carbide (SiC) is one such semiconductor.

Due to the high critical electric field for breakdown in SiC (compared to silicon) a power device with a given voltage rating can be fabricated using a drift-region whose doping is much higher than that in silicon [3]. Hence the on-resistance in SiC power devices will be much lower than that in silicon power devices, for the same voltage-rating. In 1983 Baliga [4] derived a figure of merit

$$BFOM = \varepsilon \mu E_G^3 \qquad (1)$$

which defines material parameters to minimize conduction losses in power FETs. Here ε is the dielectric constant, μ is the mobility and E_G is the band-gap of the semiconductor. Table 1 gives some of the electrical and material parameters of Si, 6H-SiC, 4H-SiC and diamond for power device applications [3,5-7]. From these values and equation 1 it can be seen that FETs made using SiC and diamond will have lower on-state losses than silicon FETs. Good quality epitaxial layers of 6H-SiC and 4H-SiC are commercially available at present. The FET structures on these materials need to be investigated. This is the aim of the present work.

Property	Silicon	6H-SiC	4H-SiC	Diamond
Band-gap (eV)	1.1	2.86	3.2	5.5
electron mobility (cm^2/V-s)	1400	84*	1140*	1870
hole mobility (cm^2/V-s)	600	99	108	250
break down electric field	$3x10^5$V/cm	$5x10^6$V/cm	$5x10^6$V/cm	$7x10^6$V/cm
dielectric constant	11.8	9.7	9.7	11.9

*these values are for mobility along the c-axis.

Table 1 : Material parameters for silicon, silicon carbide and diamond.

The contents of the sections to follow are briefly described in the following paragraphs. A first order analysis, to determine the voltage-ratings up to which unipolar devices have lower forward voltage drop than bipolar devices, is performed in section **II**. The forward voltage drops of 4H-SiC unipolar devices are compared to the forward voltage drops of silicon bipolar devices for voltage-ratings ranging from 500 V - 40,000 V

at different temperatures of operation. Similar analysis is performed for 6H-SiC unipolar and silicon bipolar devices, 4H-SiC unipolar and 4H-SiC unipolar devices and 6H-SiC unipolar and 6H-SiC bipolar devices.

In section **III**, problems associated with the operation of a SiC MOSFET and alternatives to the MOSFET are considered. The performance of a 1000 V 4H-SiC U-MESFET was studied using numerical simulations and the results are presented. Problems associated in fabricating the U-MESFET structure are discussed. In addition, a novel trench-gate heterojunction FET (HJFET) structure, with a six mask level process sequence for fabrication, is analyzed. A process sequence for fabrication of 4H-SiC and 6H-SiC HJFETs and the problems encountered during the fabrication are discussed in detail. The results of the experimental measurements are discussed and suggestions for future work on the HJFET are outlined. Each section is self contained with its own figures, tables and references.

In section **IV**, a novel planar lateral channel SiC high power JFET is described. Two-dimensional numerical simulations predicted low on-resistances with excellent current saturation and square FBSOA, which have been experimentally confirmed. In section **V**, a novel planar lateral channel SiC MESFET structure with vertical current flow in the drift region is also proposed and demonstrated by modeling and fabrication. In section **VI**, a novel planar accumulation channel SiC MOSFET structure is reported. The problems of gate oxide rupture and poor channel conductance previously reported in SiC UMOSFETs are solved by using a buried P+ layer to shield the channel region. The fabricated 6H-SiC unterminated devices had a blocking voltage of 350 V with a specific on-resistance of 18 $m\Omega$-cm^2 at room temperature for a gate bias of only 5 V. This measured specific on-resistance is within 2.5X of the value calculated for the epitaxial drift region (10^{16} cm^{-3}, 10 μm), which is capable of supporting 1500 V. In section **VII**, 6H-SiC and 4H-SiC high voltage planar ACCUFETs are compared. Section **VIII** describes the design and development of process routes leading to 4" diameter SiC substrates.

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II. First Order Analysis of Unipolar Versus Bipolar SiC Devices

A. Introduction

Silicon Carbide (SiC) has been shown to be an excellent semiconductor for the development of high voltage, high temperature and high frequency devices. The intrinsic carrier concentration in SiC is extremely low due to its large band gap compared to silicon. This enables devices fabricated from SiC to be operated at a much higher temperature than devices fabricated from silicon. Also SiC has a high critical electric field for breakdown compared to silicon. This allows the use of much higher doping and thinner epi-layers for a given breakdown voltage than is required in Si devices, resulting in much lower specific on-resistances for unipolar power devices [1].

Power devices can be broadly classified into unipolar and bipolar devices. In unipolar devices the on-state voltage drop is determined by the resistance of the drift region. The forward conduction losses are therefore determined by the drift region doping and thickness and hence increase with the voltage rating of the device. The power MOSFET is a commonly used unipolar device. In bipolar devices, on-state conduction occurs by injection of carriers across a p-n junction resulting in conductivity modulation of the drift-region. Consequently, the on-state voltage drop is determined by the contact potential of the p-n junction, because the voltage drop across the drift-region becomes small. The IGBT is the most commonly used high voltage MOS gated bipolar device. In case of the IGBT, assuming minority carrier life-times are high, the forward conduction losses are largely determined by the contact potential (V_{bi}) of the p-n junction and remain fairly constant over a large range of breakdown voltage ratings.

B. Objective of the first order analysis

For relatively small voltage ratings, thin epi-layers with high doping are needed and the voltage drop across the drift region is much lower than the contact potential. Hence it is advantageous to use unipolar devices for these applications. For higher voltage ratings, thicker low doped layers are used and the drift region drop becomes large compared to the contact potential. In bipolar devices, there is conductivity modulation of the drift-region, due to injection of minority carriers across the p-n junction, this results in a nearly constant forward voltage drop independent of the drift-region doping or thickness. Hence bipolar devices have lower on-state voltage drops than unipolar devices at high voltage ratings.

For unipolar devices, taking into account only the drift-region resistance the forward voltage drop can is given by:

$$V = \frac{JW_{C,PP}}{q\mu_n N} \qquad (1)$$

where J is the current density in the on-state, q is the electron charge, N is the doping of the material, μ_n is the electron mobility, $W_{C,pp}$ is the drift-region width [2]. The electron

mobility decreases as the temperature of operation increases: $\mu_n \alpha (T/300)^{-2.42}$ for silicon and $\mu_n \alpha (T/300)^{-1.8}$ for SiC [2,3]. Hence, the forward voltage drop for a unipolar device increases with increase in temperature. In bipolar devices, since V_{bi} decreases with temperature, the forward voltage drop actually decreases with temperature. Thus unipolar devices are suitable for low voltage and low temperature applications and bipolar devices are better suited for higher voltages and temperatures.

In general, unipolar devices are preferred over bipolar devices, due to their superior switching characteristics and safe-operating area (SOA) [2]. For silicon power devices, unipolar devices (power MOSFETs) are used for voltage ratings up to 200 V and bipolar devices are used for higher voltage ratings, in order to keep the on-state losses to a minimum. For a given voltage rating, SiC unipolar devices have a much lower specific on-resistance (about 200 times lesser) than silicon unipolar devices [1]. Hence, SiC unipolar devices can be used for much higher voltage ratings than Si unipolar devices. The forward voltage drop in bipolar devices depends on the band-gap of the material (increases with increasing band gap) and is fairly independent of the voltage rating of the device due to conductivity modulation of the drift-region. Hence, silicon (E_g = 1.1 eV) bipolar devices will always have a lower forward voltage drop than 6H-SiC (E_g = 2.86 eV) or 4H-SiC (E_g = 3.2 eV) bipolar devices. Typical on-state J-V characteristics for silicon, 6H-SiC, 4H-SiC IGBTs are shown in figure 1. Silicon has the lowest band-gap and hence silicon IGBTs have lower forward voltage drops than 6H-SiC or 4H-SiC IGBTs. The objective of this analysis is to determine the voltage rating above which the forward voltage drop of SiC unipolar devices exceeds that of silicon bipolar devices and SiC bipolar devices.

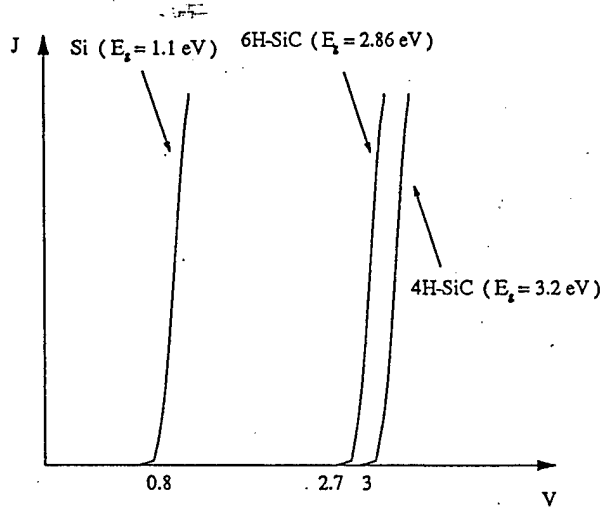

Fig.1 : Typical Forward J-V characteristics for Si, 6H-SiC, 4H-SiC IGBTs, the forward voltage drop for the silicon IGBT is the lowest.

C. Analysis

For a simple first order analysis, the forward voltage drop of a unipolar device can be assumed to be the same as the drift-region voltage drop and the forward voltage drop is given by equation 1.

The forward voltage drop of a bipolar device can be assumed to be the same as that for a P-I-N rectifier and the forward voltage drop is given by:

$$V = \frac{2kT}{q} \ln\left(\frac{Jd}{2qD_a n_i F(d / L_a)}\right) \qquad (2)$$

where n_i is the intrinsic carrier concentration, D_a is the ambipolar diffusion coefficient, L_a is the ambipolar diffusion length and d is $W_{C,PP}/2$. For this analysis, it is assumed that the minority carrier lifetimes are high enough such that $L_a = d$, i.e. $F(d / L_a)$ has its maximum value of 0.3 [2].

C.1. Analysis of cross-over current density

Figure 2 shows the typical forward J-V characteristics of a unipolar and bipolar device at two different voltage ratings. The current density at the point at which the two curves intersect will be defined as cross-over current density (J_C). J_C depends on the voltage rating of the device. As the voltage rating of the device increases, the drift-region doping decreases. This results in an increase in the forward voltage drop for unipolar devices. In case of bipolar devices, due to conductivity modulation of the drift-region the increase in forward voltage drop is much smaller. Thus, the J-V curves for unipolar and bipolar devices intersect at a lower value of current density as the voltage-rating of the device increases, as illustrated in figure 2 (i.e. $J_{C2} < J_{C1}$). For a given voltage rating, if the operating current density in the on-state is greater than J_C then a bipolar device will have a lower on-state voltage drop. If a device needs to be operated at a current density below J_C at a given voltage-rating then a unipolar device is preferred.

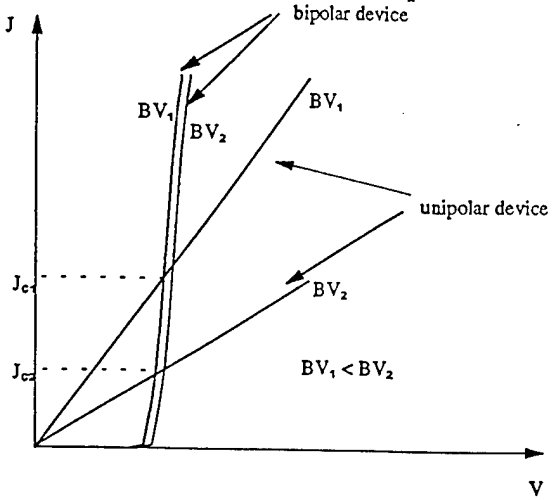

Fig. 2 : Typical Forward J-V characteristics for unipolar and bipolar devices showing the cross-over current density (J_C). J_C decreases as the breakdown voltage of the device increases.

For a given breakdown voltage rating (BV_{PP}) and temperature (T), the value of J_C can be extracted from equations (1) and (2) by equating their right hand sides and solving for J_C. The variations of N, $W_{C,PP}$ with the breakdown voltage (BV_{PP}) for SiC and silicon are given in table-1 [4-6]. The variation of the mobility with doping and temperature are also given in this table. Using these relations, J_C was calculated for 4H-SiC unipolar devices and silicon bipolar devices for voltage ratings varying from 500 V to 40000 V and temperatures of 300 K, 400 K and 500 K. Figure 3 shows the plot of J_C versus BV_{PP} for 4H-SiC unipolar and silicon bipolar devices for 3 different temperatures of operation. Figure 4 shows a similar plot for 6H-SiC unipolar and silicon bipolar devices. Plots comparing 4H-SiC unipolar devices to 4H-SiC bipolar devices and 6H-SiC unipolar devices to 6H-SiC bipolar devices are shown in figures 5 and 6, respectively. At a given temperature, J_C is a function of BV_{PP}, the variation of J_C with BV_{PP} can be determined from the curves shown in these figures or by using the relations given in table 2.

The analysis indicates that the cross-over current density for 4H-SiC unipolar and silicon bipolar devices reaches 100 A / cm^2 at approximately 4500 V at 300 K. Thus for room temperature operation, if the operating current density $\leq$ 100 A / cm^2, 4H-SiC unipolar devices will have a lower forward voltage drop than silicon bipolar devices for voltage-ratings up to 4500 V. The cross-over current density for 4H-SiC unipolar and 4H-SiC bipolar devices reaches 100 A / cm^2 at approximately 7000 V at 300 K. Thus for room temperature operation, for current densities $\leq$ 100 A / cm^2 , 4H-SiC unipolar devices will have a lower forward voltage drop than 4H-SiC bipolar devices for voltage-ratings up to 7000 V.

	silicon	4H-SiC	6H-SiC
Band-gap (E_g)	1.1 eV	3.2 eV	2.86 eV
n_i (at 300 K)	1.4×10^{10}	1.1×10^{-8}	7.6×10^{-6}

Table 1 (a)

Silicon

Doping : $N = 2 \times 10^{18} (BV_{PP})^{-4/3}$

Depletion Width at break down : $W_{C,PP} = 2.58 \times 10^{-6} (BV_{PP})^{7/6}$

Electron Mobility : $$\mu_n = \frac{5.10 \times 10^{18} + 92\, N^{0.91}}{3.75 \times 10^{15} + N^{0.91}} \left(\frac{T}{300}\right)^{-2.42}$$

Hole Mobility : $$\mu_p = \frac{2.90 \times 10^{15} + 47.7\, N^{0.76}}{5.86 \times 10^{12} + N^{0.76}} \left(\frac{T}{300}\right)^{-2.2} \qquad [2]$$

Table 1 (b)

4H-SiC

Doping : $N = 2.265 \times 10^{20} (BV_{PP})^{-1.355}$

Depletion Width at break down : $W_{C,PP} = 2.1766 \times 10^{-7} (BV_{PP})^{1.1775}$

Electron Mobility : $$\mu_n = \frac{1140}{1+\left(\frac{N}{1.94 \times 10^{17}}\right)^{0.61}} \left(\frac{T}{300}\right)^{-1.8}$$

Hole Mobility : $$\mu_p = 15.9 + \frac{108}{1+\left(\frac{N}{1.76 \times 10^{19}}\right)^{0.34}} \left(\frac{T}{300}\right)^{-1.8}$$ [3, 4]

Table 1 (c)

6H-SiC

Doping : $N = 2.265 \times 10^{20} (BV_{PP})^{-1.355}$

Depletion Width at break down : $W_{C,PP} = 2.1766 \times 10^{-7} (BV_{PP})^{1.1775}$

Electron Mobility : $$\mu_n = \frac{86.46}{1+\left(\frac{N}{1.11 \times 10^{18}}\right)^{0.59}} \left(\frac{T}{300}\right)^{-1.8}$$

Hole Mobility : $$\mu_p = 6.8 + \frac{92.2}{1+\left(\frac{N}{2.1 \times 10^{19}}\right)^{0.31}} \left(\frac{T}{300}\right)^{-1.8}$$ [3, 4]

Table 1 (d)

Table 1 (a-d): Material constants used in the First Order Analysis

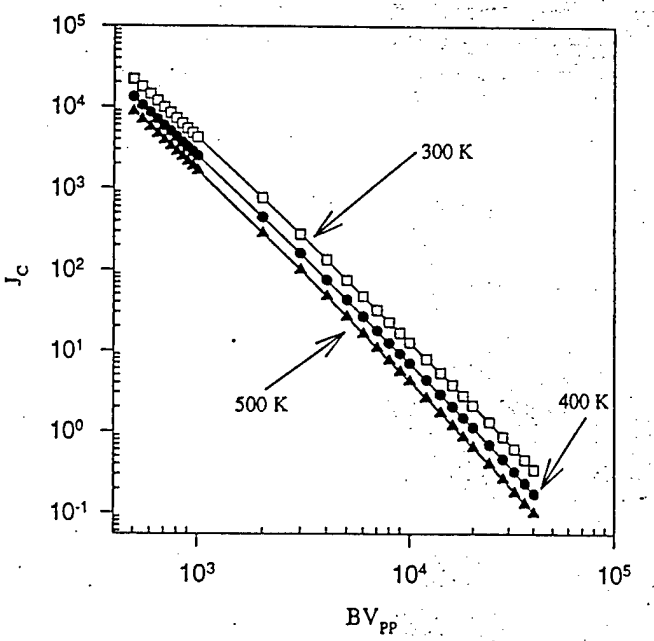

Fig. 3 : Variation of cross-over current density for 4H-SiC unipolar and Si bipolar devices with voltage-rating and temperature of operation.

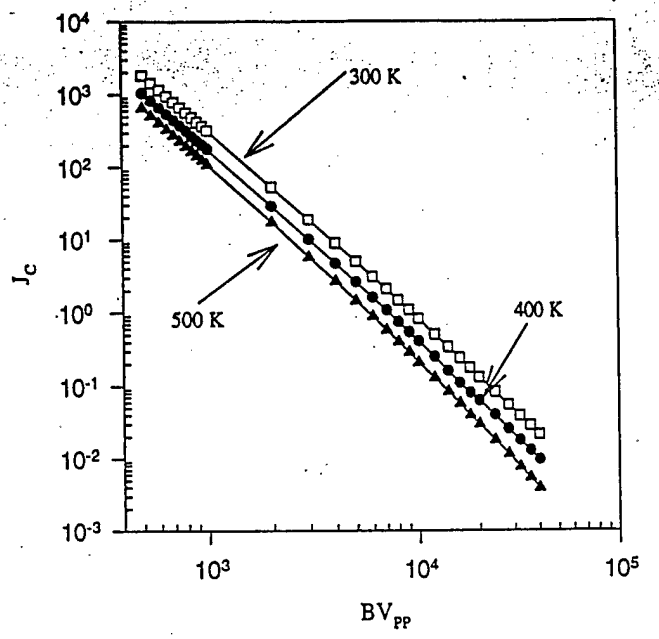

Fig. 4 : Variation of cross-over current density for 6H-SiC unipolar and Si bipolar. devices with voltage-rating and temperature of operation.

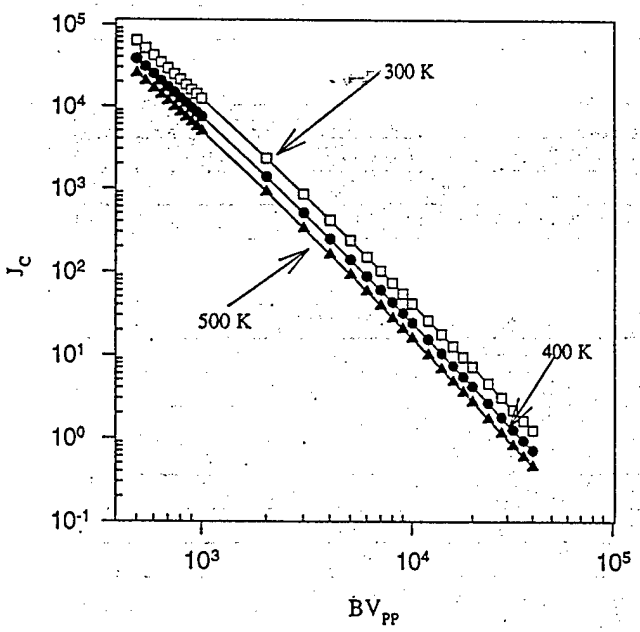

Fig. 5 : Variation of cross-over current density for 4H-SiC unipolar and bipolar devices with voltage-rating and temperature of operation..

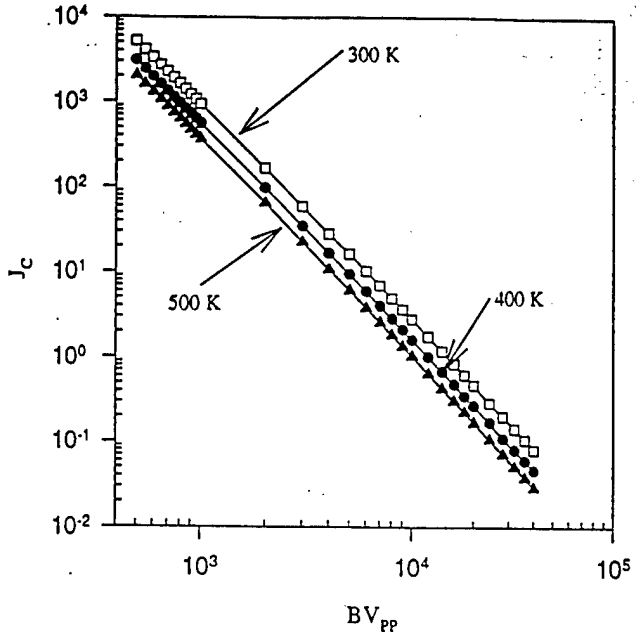

Fig. 6 : Variation of cross-over current density for 6H-SiC unipolar and 6H-SiC bipolar devices with voltage-rating and temperature of operation.

Temperature (K)	4H-SiC unipolar Vs Si bipolar
300	$J_C = 1.258 \times 10^{11} (BV_{PP})^{-2.5}$
400	$J_C = 7.76 \times 10^{10} (BV_{PP})^{-2.5}$
500	$J_C = 4.4 \times 10^{10} (BV_{PP})^{-2.5}$

(a)

Temperature (K)	6H-SiC unipolar Vs Si bipolar
300	$J_C = 1 \times 10^{10} (BV_{PP})^{-2.5}$
400	$J_C = 5.76 \times 10^{9} (BV_{PP})^{-2.5}$
500	$J_C = 3.4 \times 10^{9} (BV_{PP})^{-2.5}$

(b)

Temperature (K)	4H-SiC unipolar Vs 4H-SiC bipolar
300	$J_C = 3.7 \times 10^{11} (BV_{PP})^{-2.5}$
400	$J_C = 2.1 \times 10^{11} (BV_{PP})^{-2.5}$
500	$J_C = 1.35 \times 10^{11} (BV_{PP})^{-2.5}$

(c)

Temperature (K)	6H-SiC unipolar Vs 6H-SiC bipolar
300	$J_C = 2.9 \times 10^{10} (BV_{PP})^{-2.5}$
400	$J_C = 1.7 \times 10^{10} (BV_{PP})^{-2.5}$
500	$J_C = 1.1 \times 10^{10} (BV_{PP})^{-2.5}$

(d)

Table 2 (a-d) : Numerically derived relations for variation of cross-over current density with voltage-rating and temperature of operation for unipolar and bipolar devices.

C.2. Analysis of forward voltage drop at 100 A / cm^2

The forward voltage drop (V_F) for a unipolar device and bipolar device, for a given voltage rating (BV_{PP}), at a given current density can be calculated using equations (1) and (2) respectively. Figure 7 shows the typical variation of V_F with BV_{PP} for unipolar and bipolar devices. In unipolar devices, the forward voltage drop depends on the drift-region resistance. The drift-region resistance increases as the breakdown voltage increases, since the doping decreases resulting in a gradual increase in the forward voltage drop with the voltage-rating of the device. In bipolar devices there is conductivity modulation of the drift-region and the forward voltage drop is nearly the same for all voltage-ratings. The voltage rating at which the two curves intersect will be defined as the cross-over breakdown voltage BV_C. For voltage ratings lesser than BV_C unipolar devices have a lower V_F than bipolar devices and for voltage ratings greater than BV_C bipolar devices have a lower V_F than unipolar devices . The forward voltage drop for 4H-SiC unipolar devices and silicon bipolar devices at a current density of 100 A / cm^2 at 3 different temperatures (300 K, 400 K, 500 K), as a function of the voltage rating (BV_{PP}) are shown in figure 8. As the temperature, increases the forward voltage drop in unipolar devices increases due to degradation of mobility while the forward voltage drop in bipolar devices decreases slightly with increase in temperature. Hence the V_F versus BV_{PP} curves for 4H-SiC unipolar devices shift up as the temperature increases whereas the curves for silicon bipolar devices remain nearly unchanged. It can be seen that at 300 K, the value of BV_C is approximately 4500 V. This implies that 4H-SiC unipolar devices have a lower V_F than silicon bipolar devices for voltage ratings upto 4500 V. Figure 9 shows a similar plot for 6H-SiC unipolar devices and silicon bipolar devices. The cross-over breakdown voltage in this case is approximately 1000 V as against 4500 V in the previous case. This is due to the fact that the electron mobility along the c-axis in 6H-SiC is nearly 10 times lower than that in 4H-SiC. Similar plots for 4H-SiC unipolar and 4H-SiC bipolar devices are shown in figure 10 and the value of BV_C at 300 K is approximately 7000 V. Figure 11 shows a similar plot for 6H-SiC unipolar and 6H-SiC bipolar devices. The values of BV_C at different temperatures are given in table 3.

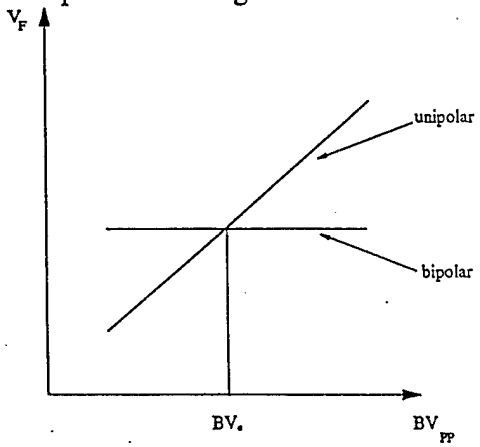

Fig. 7 : Typical variation of forward voltage drop (V_F) with the voltage-rating (BV_{PP}) for unipolar and bipolar devices, the voltage-rating at which the two curves intersect is called the cross over breakdown voltage (BV_C).

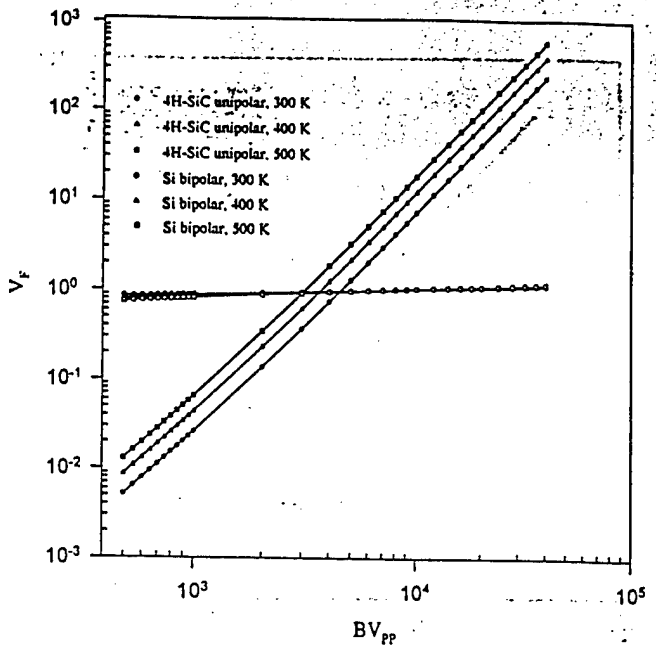

Fig. 8 : Variation of V_F (at 100 A / cm^2) with voltage-rating for 4H-SiC unipolar and silicon bipolar devices at 3 different temperatures.

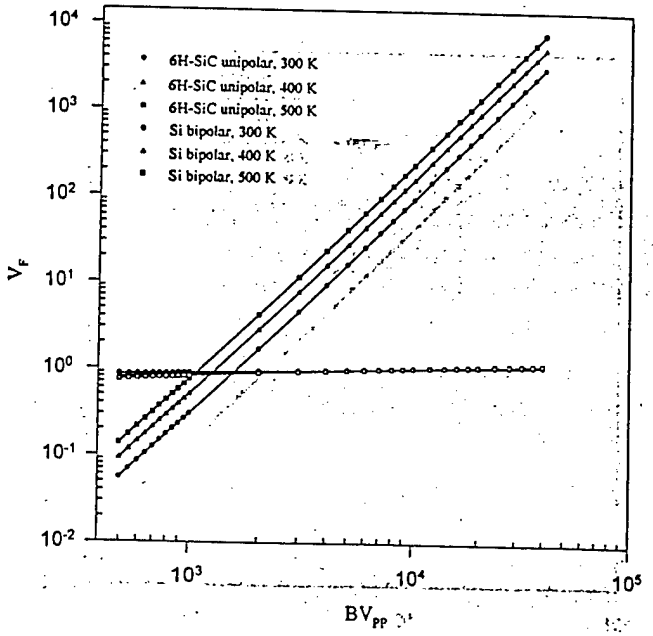

Fig. 9 : Variation of V_F (at 100 A / cm^2) with voltage-rating for 6H-SiC unipolar and silicon bipolar devices at 3 different temperatures.

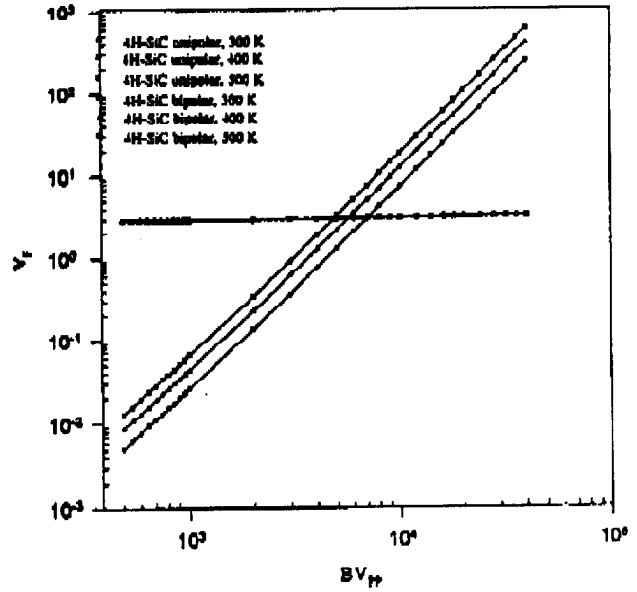

Fig. 10 : Variation of V_F (at 100 A / cm^2) with voltage-rating for 4H-SiC unipolar and 4H-SiC bipolar devices at 3 different temperatures.

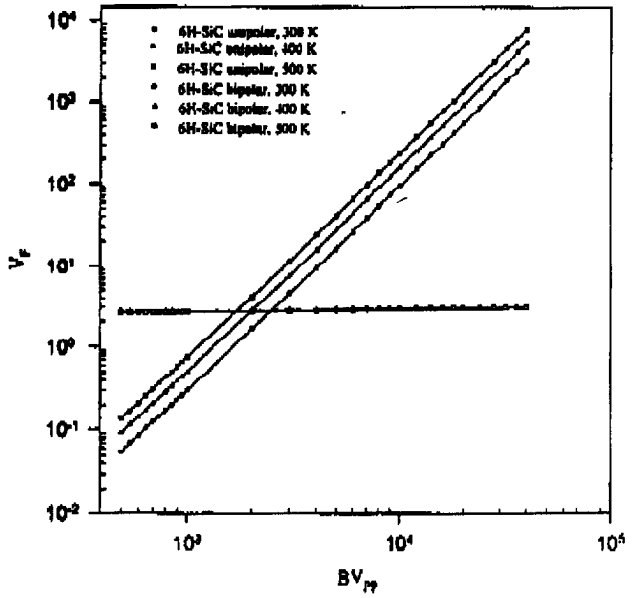

Fig. 11 : Variation of V_F (at 100 A / cm^2) with voltage-rating for 6H-SiC unipolar and 6H-SiC bipolar devices at 3 different temperatures.

Material / Temperature	4H-SiC / Si	6H-SiC / Si	4H-SiC/4H-SiC	6H-SiC/6H-SiC
300 K	4500 V	1800 V	7000 V	2500 V
400 K	3500 V	1200 V	5500 V	2000 V
500 K	3000 V	1050 V	4500 V	1800 V

Table 3 : Cross-over breakdown voltages for unipolar Vs bipolar devices for 4H-SiC, 6H-SiC, Si at different temperatures of operation.

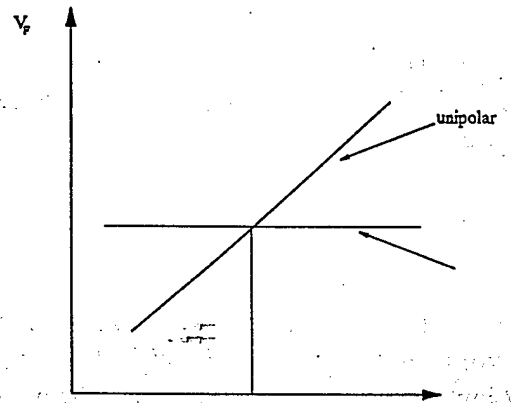

Fig. 12 : Variation of V_F with temperature for unipolar and bipolar devices, the temperature at the point of intersection of these curves is defined to be the cross-over temperature (T_C)

For a given breakdown voltage, the forward voltage drop for unipolar devices increases with temperature while that for bipolar devices decreases. Figure 12 shows a typical variation of the forward voltage drop with temperature for unipolar and bipolar devices. The temperature at which the V_F versus T curves for unipolar and bipolar devices intersect will be defined as the cross-over temperature (T_C). The values of T_C as a function of the breakdown voltage (BV_{PP}) for 4H-SiC unipolar and silicon bipolar devices are plotted in figure 13. Similar plots for 6H-SiC unipolar and silicon bipolar devices, 4H-SiC unipolar and bipolar devices, 6H-SiC unipolar and bipolar devices are also shown in the same figure. At a given voltage-rating, if the temperature of operation of the device is going to be less than T_C then a unipolar device will have a lower forward voltage drop than a bipolar device. If the temperature of operation is more than T_C then the bipolar device will have a lower forward voltage drop. The value of T_C at 3000 V for 4H-SiC unipolar devices to silicon bipolar devices is approximately 500 K. Thus for a voltage-rating of 3000 V if the temperature of operation of the device is going to be less than 500 K then 4H-SiC unipolar devices will be preferred over silicon bipolar devices as they will have a lower forward voltage drop.

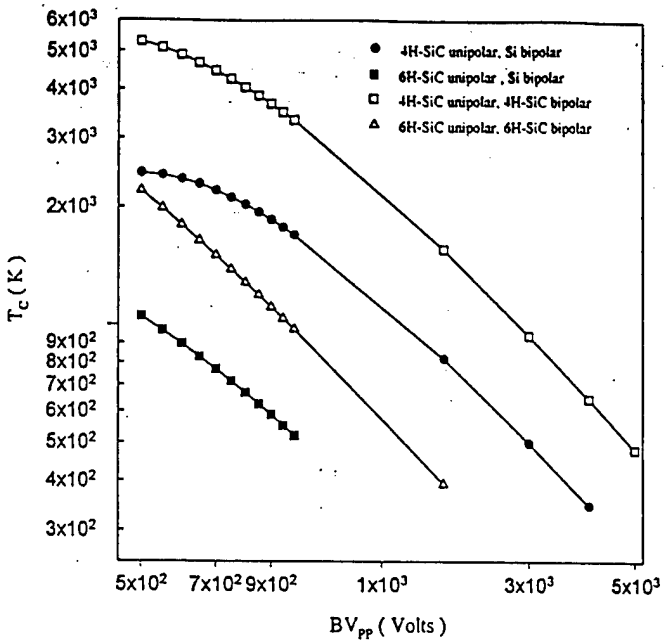

Fig. 13 : Variation of cross-over temperature with the voltage-rating of the device, if the temperature of operation is below the cross-over temperature unipolar devices have a lower V_F than bipolar devices.

D. Conclusions

A first order analysis to compare the performance of unipolar devices to bipolar devices over a range of voltage-ratings (500 V - 40000 V) was performed. The forward voltage drop at 100 A / cm^2 was used to do the comparison. It was found that for room temperature operation, 4H-SiC unipolar devices have lower forward voltage drops than silicon bipolar devices for voltage ratings upto 4500 V.

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III. Vertical Channel UMESFET

1. Analysis of the U-MESFET

A. Introduction

From the discussion in the previous section, it is evident that silicon carbide unipolar power devices are preferable for voltage ratings below 4500 V. The most commonly used unipolar device in silicon power device technology is the power MOSFET. In this section the current status of silicon carbide MOSFETs and associated problems are presented. The alternatives to the power MOSFET are the JFET and the MESFET. The output characteristics of a 1000 V silicon carbide MESFET are analyzed using simulations.

B. Background

B.1 Power MOSFET

The two commonly used MOSFET structures are the DMOSFET and the UMOSFET shown in figures 1 (a) and 1 (b) respectively. In both the MOSFET structures, the p-n junction between the P-base region and the N-drift region provides the blocking capability. Due to the very small diffusion rate of dopants in silicon carbide, it is not practical to fabricate the DMOSFET [1]. The most suitable structure is the U-MOSFET in which the P-base region is epitaxial grown on the N-drift layer. The power MOSFET is capable of blocking voltage in only one quadrant. For n-channel structures the devices are operated with a positive voltage applied to the drain. When the gate electrode is shorted to the source the device can support a large drain voltage across the P-base/N-drift region junction. The forward blocking capability is shown in figure 2 by the lowest trace [2].

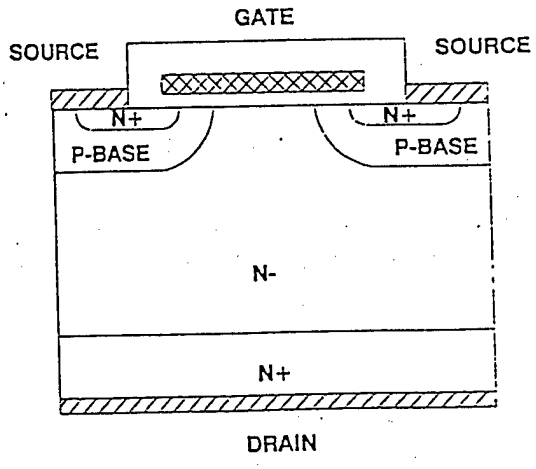

Fig.1 (a) : Cross Section Of a D-MOSFET

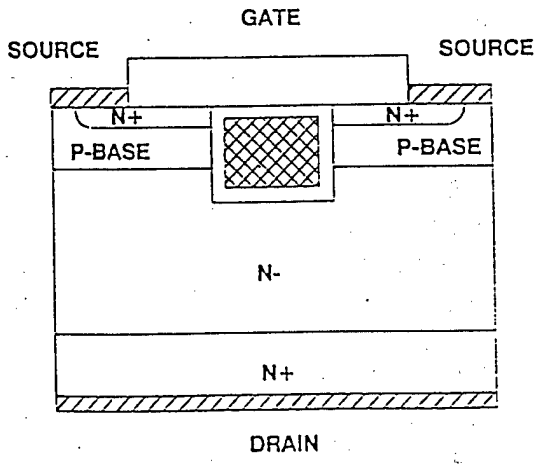

Fig. 1 (b) : Cross Section Of a U-MOSFET

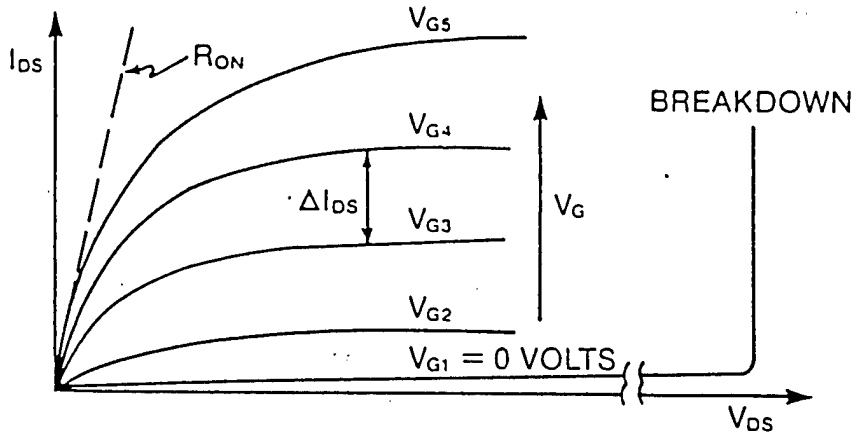

Fig. 2 : Output characteristics of a typical MOSFET, the forward blocking capability is shown by the lowest trace.

When a positive gate bias is applied, the channel becomes conductive. At low drain voltages the current flow is resistive with the on-resistance determined by a combination of the channel and drift region resistances. The total on-resistance decreases with increasing gate-bias until it approaches a constant value. At high drain voltages, the resistance of the power MOSFET increases and ultimately the current saturates at high drain voltages as shown in figure 2.

B.2.Problems with SiC MOSFETs

The UMOSFET on-resistance consists mainly of the channel resistance and the drift-region resistance[2]. The channel resistance ($R_{ch,sp}$) is given by :

$$R_{ch,sp} = \frac{L_{ch} (W_m + W_t)}{2 \mu_{ns} C_{ox} (V_G - V_T)} \qquad (1)$$

where L_{ch} is the length of the channel, W_m and W_t are the trench and mesa-widths respectively, C_{ox} is the capacitance per unit area of the gate oxide, V_G and V_T are the gate and threshold voltages and μ_{ns} is the inversion channel mobility [2]. In order to achieve an on-resistance value close to the ideal value, the channel resistance should be made as low as possible. Hence it is important to obtain a high inversion channel mobility.

The inversion channel mobilities reported in silicon carbide are very low (20 cm^2/V-s) [3], resulting in severe degradation of specific on-resistances. This is illustrated in figure 3 where the calculated specific on-resistance is given as a function of the breakdown voltage for various inversion layer mobility values [1]. Further the critical electric field for breakdown in silicon carbide is approximately 5 x 10^6 V/cm and since the field in the oxide will be about thrice the field in the underlying silicon carbide, the electric field in the oxide can reach its breakdown strength of 1 x 10^7 V/cm at the trench corners, as shown in figure 4, leading to rupture of the gate oxide and premature breakdown of the

device[1]. Due to these problems, MOSFETs cannot be used to realize the potential of silicon carbide as a superior replacement to silicon. Hence, it is important to investigate other unipolar structures like the JFET and the MESFET shown in figures 5 (a) and 5(b) respectively. However the fabrication of a SiC JFET is impractical due to the high energies required to implant the p^+ gate. The MESFET needs a good Schottky contact to be formed between the metal and semiconductor in order to achieve good forward blocking. Schottky rectifiers with high blocking capabilities (400 V-1000 V) and reasonably low leakage currents have been reported on both 4H-SiC and 6H-SiC [4-6]. Hence the vertical MESFET (U-MESFET) structure was chosen for investigation.

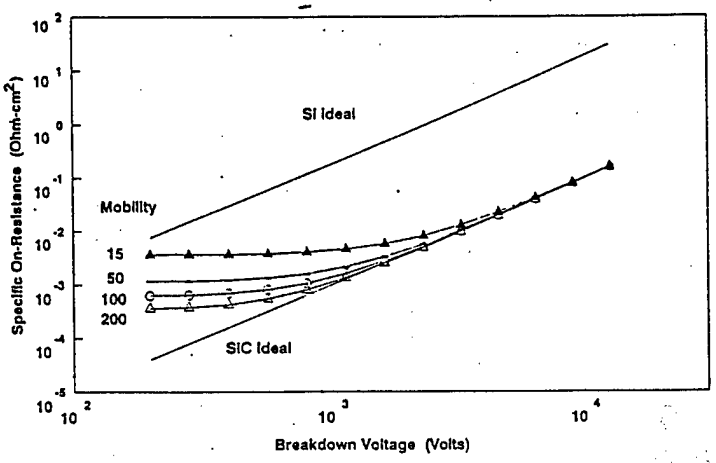

Fig. 3 : Variation of Specific On-resistance with breakdown voltage and inversion layer mobilities for a SiC MOSFET.

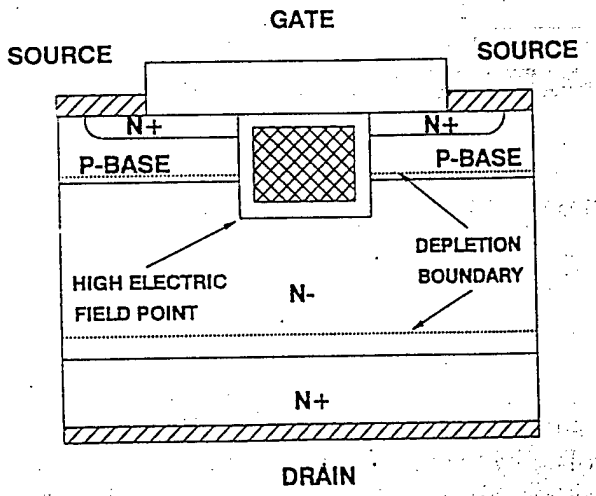

Fig.4 : Electric Field Crowding at the trench corner in a SiC U-MOSFET can cause premature breakdown of the oxide layer.

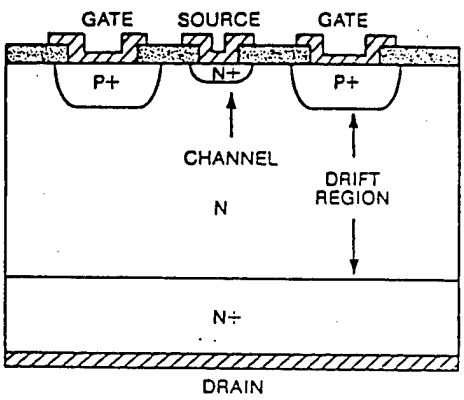

Fig. 5 (a) : Cross Section Of a JFET, the gate is formed by P^+diffusion or implant into the N-epilayer.

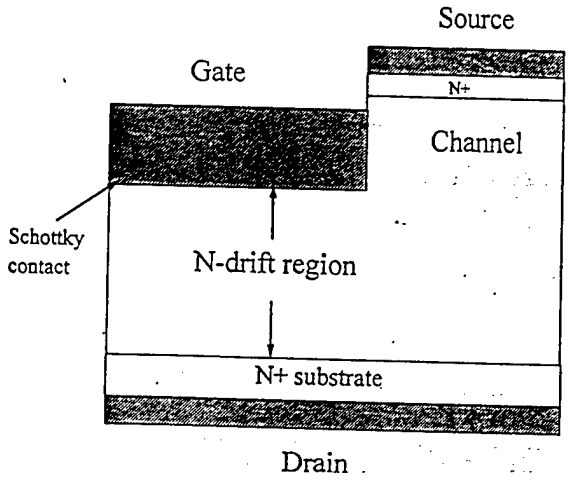

Fig. 5 (b) : Cross-section of a U-MESFET, the Schottky gate is formed in a trench.

C. U-MESFET

C.1 Basic Operation

Fundamentally, the MESFET consists of a bar of semiconductor material whose resistance can be controlled by the application of a reverse-bias voltage to a gate region. A U-MESFET (metal-semiconductor field effect transistor) is shown in figure 5 (b). The gate is a Schottky junction, formed in a trench in order to isolate it from the source. In the absence of a gate bias, that is, with the gate short-circuited to the source, the current flow between drain and source is limited by the resistance of the lightly doped N-type region

between these current carrying terminals. The N-type region consists of two portions, the region between the junction gates is called the channel and the region below the junction gates is called the drift region. The resistances of both these regions add together to determine the total resistance to current flow between the drain and source terminals.

With the application of a reverse gate bias with respect to the source (negative voltage to the gate terminal), a depletion region forms around the gate junctions and extends out into the channel. Since the depletion region is devoid of free carriers, the resistance of the channel region increases with the application of higher reverse gate bias voltages. By use of the gate junction depletion layer, the resistance of the MESFET can be altered by changing the reverse gate bias voltage. Thus, the MESFET is a voltage-controlled device. In the MESFET, the gate bias supply needs to provide only a small displacement current to modulate the depletion region width, resulting in a high input impedance.

C.2 Forward Blocking

The resistance of the MESFET is controlled by changing the channel conductivity. In a MESFET designed for operation at high drain voltages, it is necessary to include a wide drift-region. During the application of large drain voltages in the forward blocking mode, the voltage is supported across the gate depletion layer. This depletion layer extends down from the gate junction toward the drain. The drift region doping concentration and thickness should be designed to support the drain-gate voltage, that is, the sum of the absolute values of the drain and gate voltages, because they combine to determine the total reverse bias across the gate Schottky junction. It should also be noted that the gate-source structure must be capable of supporting the highest gate-source voltage.

In the forward blocking mode, the depletion layers from the gate junctions extend through the entire channel. The applied reverse gate bias sets up a potential barrier in the channel. For current to flow between drain and source, electrons must surmount this potential barrier. As the drain voltage increases the potential barrier is lowered and electron injection becomes easier [7].

C.2.1 Triode like characteristics of the U-MESFET

The channel length in a U-MESFET is determined by the depth of the trench. In silicon carbide, due to the slow etch rates, the practical trench-depths are ≤ 3 μm. Thus for a silicon carbide U-MESFET, the channel length would be typically the same as the channel width. For these devices, the potential barrier established in the channel by the reverse gate bias extends over only a small vertical distance. As the drain voltage is increased, the drain potential penetrates into the channel and lowers the potential barrier. At low drain voltages, the potential barrier established by the gate voltage is pronounced and extends throughout the channel. When the drain voltage is increased, the potential barrier is pulled down by the drain potential in regions of the channel away from the gate region. Electron injection can now occur in these regions. Since the injection of carriers across the potential barrier varies exponentially with the barrier height, the drain current exhibits a rapid increase once the potential barrier is reduced. The resulting triode like

characteristics, that is, drain current continuously increasing with increasing drain voltage, of MESFETs with short channel length are illustrated in figure 6. [7].

C.2.2 Blocking Gain

An important parameter for devices with triode like characteristics is the voltage blocking gain. The DC blocking gain can be defined as

$$G_B = \frac{V_{DS}}{V_{GS}} \qquad (2)$$

where V_{DS} is the maximum voltage blocked by a gate-bias V_{GS}. It is crucial to achieve a large blocking gain in high-voltage MESFETs for two reasons : (1) a higher blocking gain reduces the gate drive voltage that must be supplied by the gating circuit to achieve any desired forward blocking capability, and (2) a higher blocking gain reduces the total voltage that must be supported by the gate junction. The total reverse bias across the gate junction is given by

$$V_{RJ} = (V_{DS} + V_{GS}) = V_{DS}\,(1+\frac{1}{G_B}) \qquad (3)$$

A large blocking gain reduces the breakdown voltage that must be designed for the gate junctions.

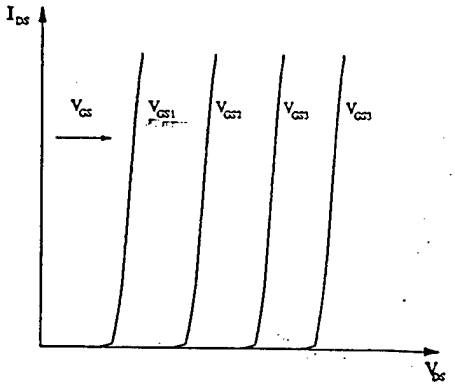

Fig. 6 : Triode like Output Characteristics Of the MESFET.

C.2.3 Forward Conduction, On-Resistance

The U-MESFET is a normally-on device and conducts current through the channel when a positive bias is applied to the drain with all the other terminals at zero bias. The on-resistance of the U-MESFET is the resistance between the source and drain terminals in the on-state. The on-resistance is an important device parameter because it determines the maximum current rating. The power dissipation in the U-MESFET, during the on-state is given by:

$$P_D = I_D V_D = I_D^2 R_{on} \qquad (4)$$

Expressed in terms of the chip area (A):

$$\frac{P_D}{A} = J_D^2 R_{on,sp} \qquad (5)$$

where (P_D / A) is the power dissipation per unit area; J_D is the on-state current density; and $R_{on,sp}$ is the *specific on-resistance*, defined as the on-resistance per unit area. For a given power dissipation the operating current density varies inversely as the square root of the specific on-resistance [2].

The specific on-resistance of the power U-MESFET is determined by the resistance components illustrated in figure 7 for the U-MESFET structure. Thus:

$$R_{on} = R_{CS} + R_{N^+} + R_R + R_J + R_D + R_S + R_{CD} \qquad (6)$$

where R_{N+} is the contribution from the N^+ source implant, R_R is the resistive component just under the source implant, R_J is the contribution from the drift region between the Schottky gates, R_D is the drift region resistance and R_S is the substrate resistance. Additional resistances can arise from non-ideal contact (R_{CS} and R_{CD}) between the source/drain metal and the N^+ semiconductor regions as well as the leads used to connect the device to the package. Each of these contributions is described below.

Substrate resistance: The contribution from the substrate is generally negligible for high-voltage MESFETs. It can be assumed that the current density is uniform within the substrate because of rapid current spreading at the drift region interface. The specific on-resistance contributed by the substrate is then given by:

$$R_{S,sp} = \rho_s t_s \qquad (7)$$

where ρ_s is the resistivity of the substrate and t_s is its thickness. Typically $R_{S,sp}$ is of the order of $1x10^{-4}$ Ω-cm^2.

Source Resistance: The resistance per cm^2 due to the N^+ source is given by:

$$R_{N+,sp} = \frac{\rho_{N+} L_{N+} (Wt + W_m)}{W_m} \qquad (8)$$

where ρ_{N+} is the sheet resistance of the N^+ source, L_{N+} is the thickness of the N^+ contact region, W_t is the trench-width and W_m is the mesa-width as shown in figure 7. Typically $R_{N+,sp}$ is of the order of 1×10^{-7} Ω-cm^2.

R_R is the resistance of the region under the N^+ source and just above the channel and is given by:

$$R_{R,sp} = \frac{\rho_D (t_d - L - L_{N+} - W_D)(W_t + W_m)}{W_m} \qquad (9)$$

where ρ_D is the drift region resistivity, L is the gate length and W_D is the depletion width due to contact potential of the Schottky gate. Typically $R_{R,sp}$ is in the order of $1x10^{-5}$ Ω-cm^2.

Channel Resistance :The channel resistance in U-MESFETs is similar to the JFET region resistance in the D-MOSFET [2]. The channel resistance per cm^2 for the structure shown in figure 7 is given by :

$$R_{J,sp} = \frac{\rho_D (W_t + W_m)(L + 2W_D)}{(W_m - 2W_D)} \qquad (10)$$

For $W_t = W_m = 1$ μm with the channel doping of the order of $1x10^{16}$ cm^{-3}, the channel resistance is of the order of $1x10^{-4}$ Ω-cm^2.

Drift Region Resistance: In this analysis, the drift region is assumed to begin below the bottom of the trench as indicated in figure 7. The current spreads from the channel region into the drift region. Many possible models for the current spreading into the drift region can be proposed. One such model that allows a reasonably accurate estimation of the drift region spreading resistance, is based on the current spreading from a cross-section of ($a = W_m - 2W_D$) at a 45 degree angle[8]. The current flow paths overlap at a depth $W_G / 2$ below the trench bottom and the drift region resistance can be modeled as the sum of a region where the cross-section for current flow increases with depth and a second region with uniform cross-section equal to the cell-width. This leads to a drift region specific resistance given by:

$$R_{D,sp} = \frac{\rho_D (W_t + W_m)}{2} \ln\left[\frac{W_m - 2W_D + W_t}{W_m - 2W_D}\right] + \rho_D (t - t_d - \frac{W_t}{2}) \qquad (11)$$

Typically $R_{D,sp}$ is in the order of 10^{-4} Ω-cm^2, for a voltage-rating of 1000 V.

Thus the channel resistance and drift-region resistance are the main components that determine the specific on-resistance of the U-MESFET.

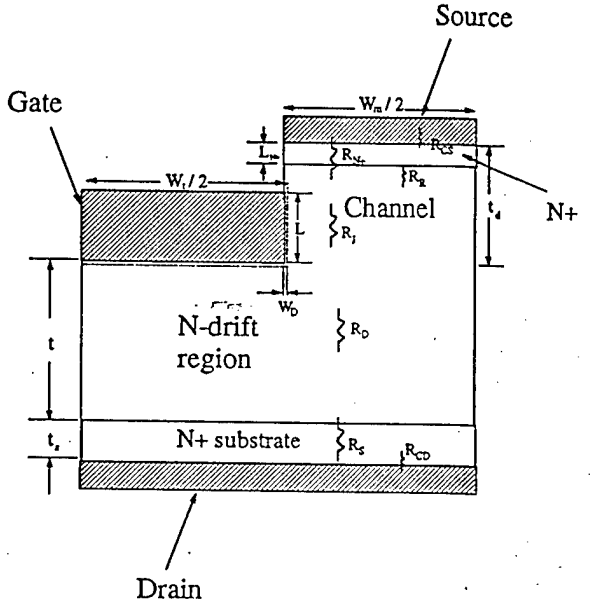

Fig. 7 : Cross Section Of the U-MESFET illustrating the various components of On-Resistance.

D. SiC U-MESFET : Numerical Simulations

Two-dimensional numerical simulations of the U-MESFET shown in figure 7 were performed using *TMA-MEDICI* to analyze the performance of the device. The electron drift mobility in 4H-SiC, along the c-axis, is nearly 10 times higher than that in 6H-SiC [9]. Hence 4H-SiC was used in the simulations as the specific on-resistance will be lower for 4H-SiC devices.

D.1 Design Variations studied using simulations

The blocking gain of the U-MESFET depends on the gate-bias needed to pinch-off the channel. A thin channel can be pinched off with a low gate-bias resulting in a high blocking gain whereas a wide channel will result in a lower blocking gain. In order to study the variation of blocking gain with the channel width, the mesa-widths (W_m) of the simulated structures was varied from 1 μm - 3 μm, the ratio W_t/W_m was fixed at 1 for all the cases. The N^- region doping was varied from $1x10^{16}$ cm^{-3} - $2x10^{16}$ cm^{-3}, the gate-length (L) was varied from 0.5 μm-1 μm and the trench-depth (t_d) was fixed at 1.5 μm. The N^+ implant for source contact was fixed at 0.2 μm . Since titanium is known to form good Schottky contact to 4H-SiC [4], the simulations were performed with titanium as the metal for the Schottky gate. This was done by specifying the work function of the metal contact to be 4.77 eV. A design variation with gold (work function = 5.3 eV) as the Schottky gate was also simulated, in order to study the variation of blocking gain and on-state resistance with the type of metal used to form the Schottky gate.

D.2 Variation of potential barrier in the channel

Figure 8 shows the potential barrier in the channel region for a gate bias (V_{GS}) of -20 V and a drain bias (V_{ds}) of 50 V, for the different simulated structures, with L = 1 μm and a doping of $1x10^{16}$ cm^{-3}. It can be seen that for a given gate-length, the barrier is maximum for the structure with the smallest mesa-width and decreases with increasing mesa-width. This is due to the fact that the gate-bias needed to pinch off a smaller mesa-width is smaller. A similar plot with L = 1 μm and W_m, W_t = 1 μm for two different dopings of $1x10^{16}$ cm^{-3} and $2x10^{16}$ cm^{-3} is shown in figure 9. It can be seen that the structure with lower doping has a higher potential barrier. This is due to the fact that a low doped channel can be pinched off with a smaller gate-bias. The variation of the potential barrier with the gate-length is illustrated in figure 10. It can be seen that the barrier reduces as the gate-length decreases. The variation of potential barrier in the channel for different Schottky contacts (Ti, Au) is shown in figure 11. It can be seen that the Schottky gate with gold as the metal has a higher barrier, this is due to the fact that gold forms a Schottky contact with a higher barrier height than titanium [4-5] and hence higher contact potential which results in the channel getting pinched off at a lower gate bias than that is needed for a titanium gate. Thus the gate-bias needed to turn-off the device depends on the mesa-width, gate-length, channel doping and the work function of the gate metal.

D.3 Forward Blocking Characteristics

The simulated triode-like blocking characteristics for the structures with doping of $1x10^{16}$ cm^{-3}, gate-length of 1μm, with a titanium gate, with the mesa-widths varying from 1μm to 3μm are shown in figures 12(a)-12 (d). Since the doping and epi-layer thickness is fixed for all the cases, the forward blocking voltage and the gate bias needed to achieve the blocking are determined by the potential barrier in the channel region. As is expected, the structure with the smallest mesa-width (1 μm) needs the least gate voltage (-10 V) to achieve the rated blocking voltage of 1200 V, whereas the structure with W_m = 3 μm is able to block only 350 V even with a gate-bias of -100 V.

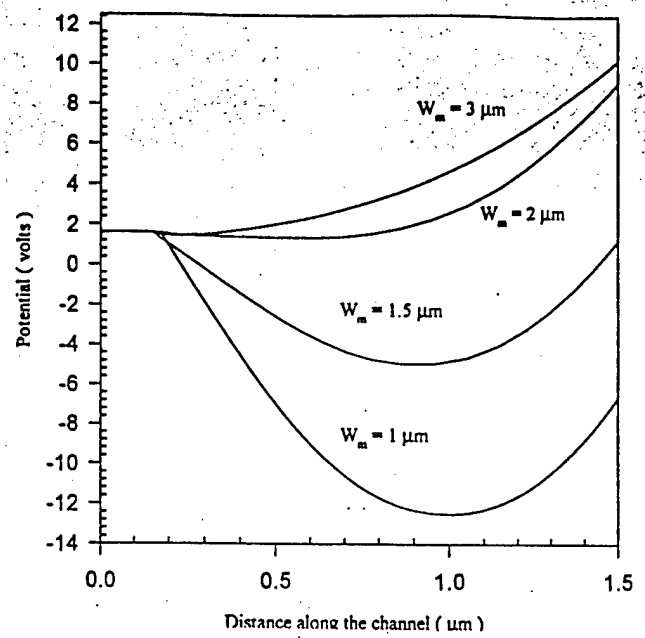

Fig. 8 : For a given doping ($1x10^{16}$ cm^{-3}) and gate-length (1 μm), the potential barrier in the channel increases as the mesa-width decreases. V_{GS} = -20 V, V_{DS} = 50 V

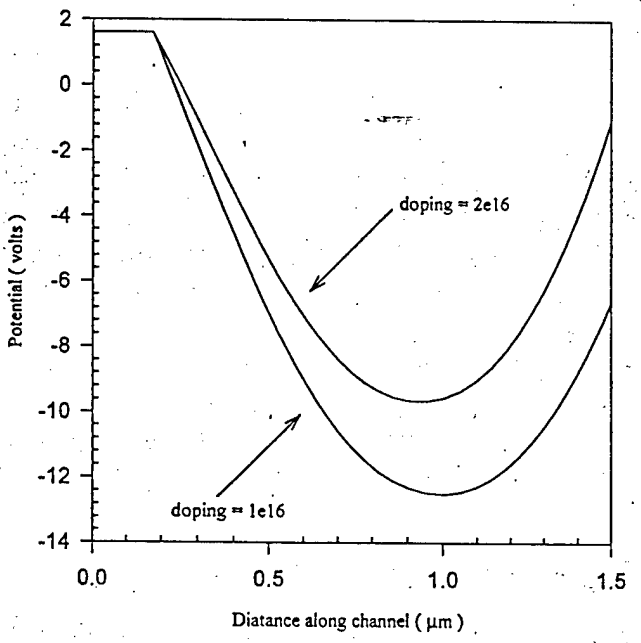

Fig. 9: For a fixed gate-length (1μm) and mesa-width (1μm) the potential barrier in the channel increases as the doping is reduced. V_{GS} = -20 V, V_{DS} = 50 V.

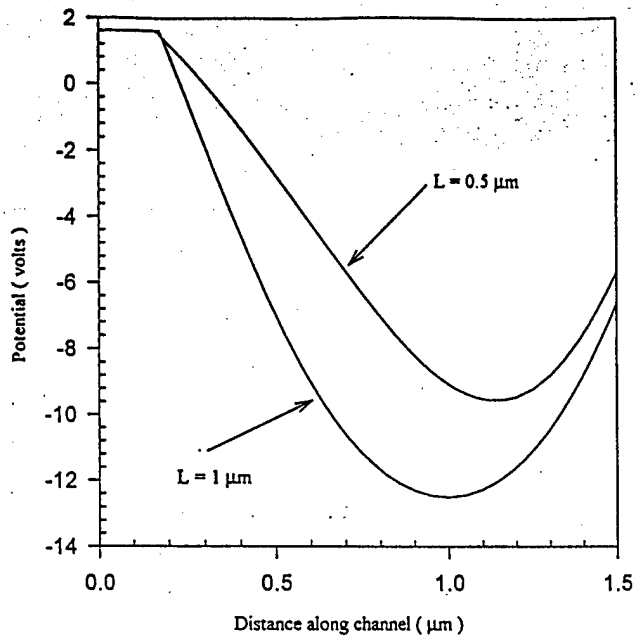

Fig. 10 : For a fixed mesa-width (1μm) and doping ($1x10^{16}$ cm^{-3}) the potential barrier in the channel decreases as the gate-length decreases. V_{GS} = -20 V, V_{DS} = 50 V.

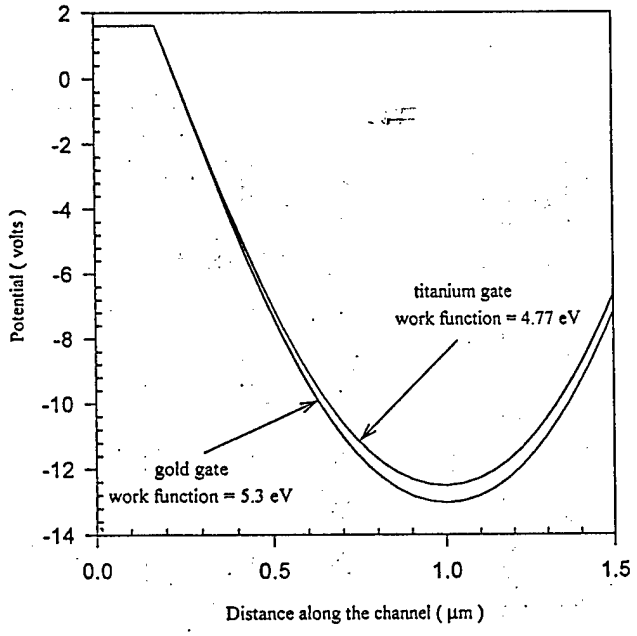

Fig. 11 : For a given mesa-width (1μm), gate-length (1μm) and doping ($1x10^{16}$ cm^{-3}) the potential barrier in the channel increases with the work function of the gate metal. V_{GS} = -20 V, V_{DS} = 50 V

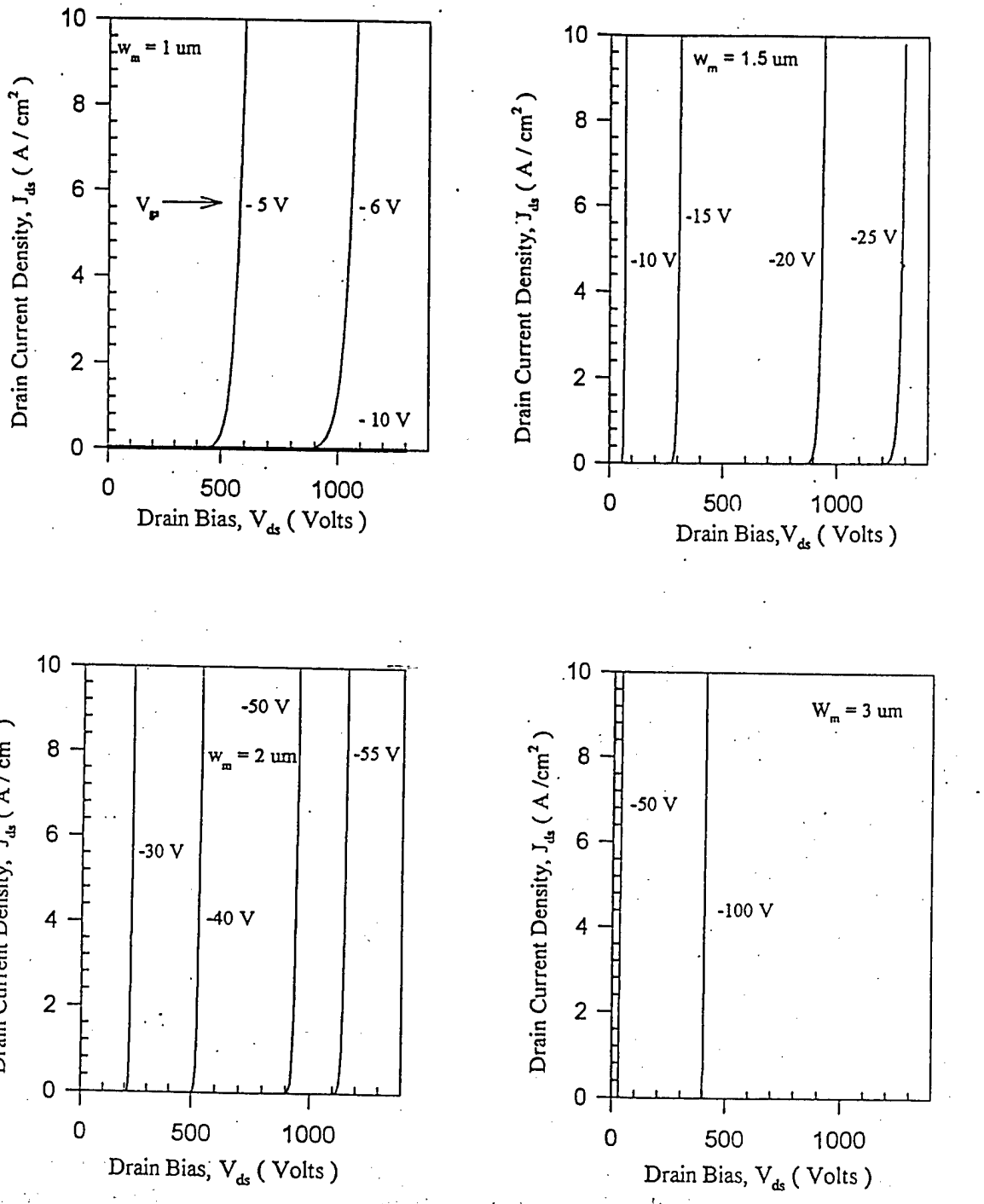

Fig.12 (a-d) : Forward blocking characteristics of the U-MESFET with different mesa-widths. The structure with the smallest mesa-width needs the lowest gate-bias to achieve the rated blocking voltage.

D.4 Electric Field Distribution

The three-dimensional electric field distributions for the structure with W_m = 1μm and W_m = 1.5 μm at a drain bias of 1200 V are shown in figure 13(a) and 13(b). It can be seen that there is electric-field crowding at the trench corners. This crowding causes premature breakdown in U-MOSFETs as the field in the oxide will be thrice that in the semiconductor [1], but the U-MESFET does not have any such problems and is able to block the rated voltage.

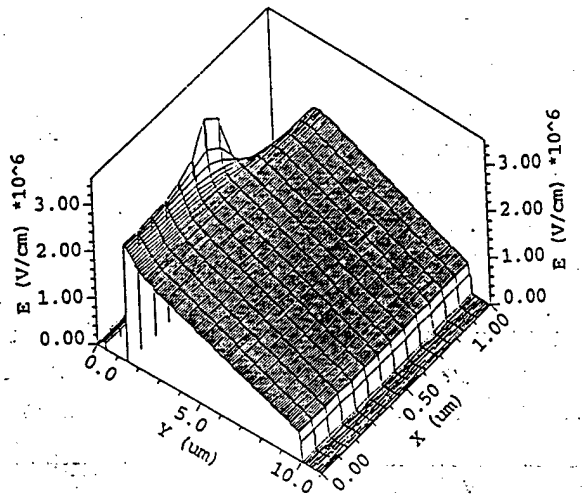

Fig. 13 (a) : Three-Dimensional Electric Field Distribution at V_{gs} =-10 V and V_{ds} = 1200 V for structure with W_m = 1 μm and doping = $1x10^{16}$ cm^{-3}

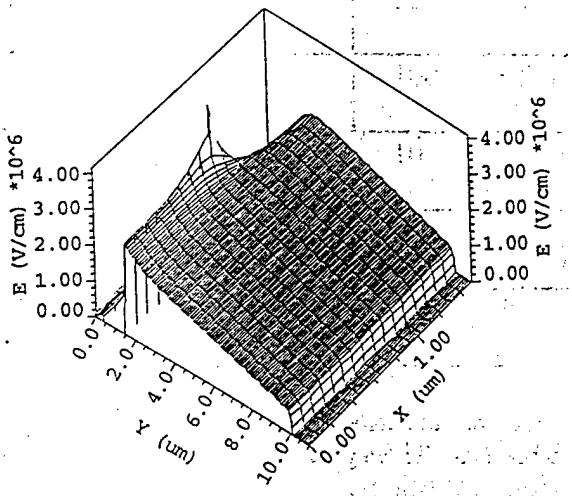

Fig. 13 (b) : Three-Dimensional Electric Field Distribution at V_{gs} =-25 V and V_{ds} = 1200 V for structure with W_m = 1.5 μm and doping = $1x10^{16}$ cm^{-3}.

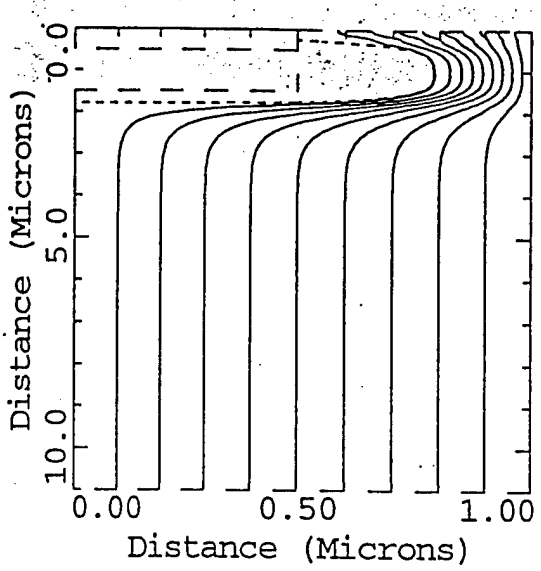

Fig. 14 (a) : $W_m = 1\ \mu m$

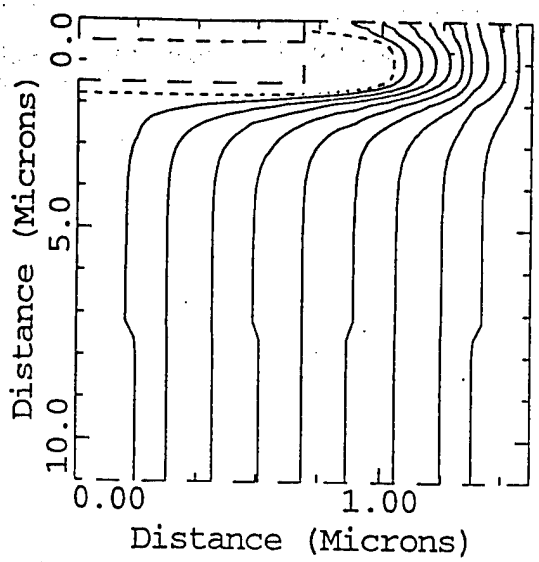

Fig. 14 (b) : $W_m = 1.5\ \mu m$

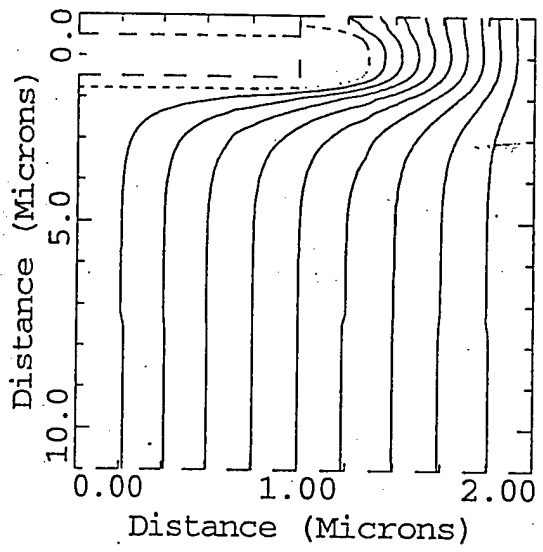

Fig. 14 (c) : $W_m = 2\ \mu m$

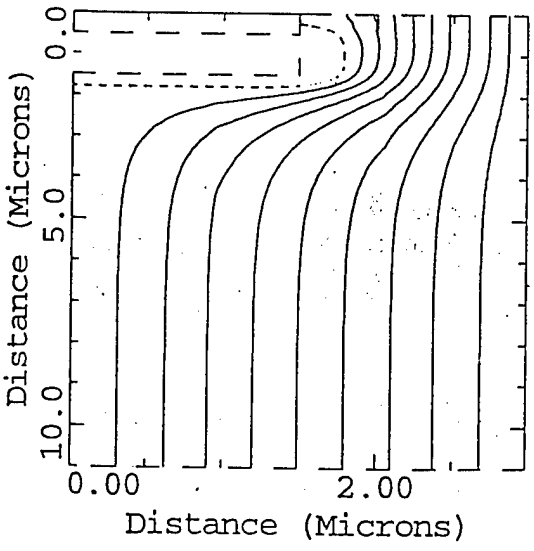

Fig. 14 (d) : $W_m = 3\ \mu m$

Fig. 14 (a-d) : The fraction of the channel depleted at zero gate-bias decreases with increasing mesa-width, resulting in lower specific on-resistance. The current flowlines spread uniformly in the drift region resulting in a low on-resistance, close to the ideal value, for all the structures. The doping for all the structures shown is 1×10^{16} cm^{-3} and the gate metal is titanium.

*Structure #	$R_{on\text{-}sp}$ (Ω-cm^2) simulated	$R_{on\text{-}sp}$ (Ω-cm^2) calculated
1	9.6×10^{-3}	1.1×10^{-3}
2	8.6×10^{-4}	9.4×10^{-4}
3	8.35×10^{-4}	8.8×10^{-4}
4	7.95×10^{-4}	8.6×10^{-4}
5	4.45×10^{-4}	4.8×10^{-4}
6	8.75×10^{-4}	9.5×10^{-4}
7	9.3×10^{-4}	9.8×10^{-4}

*Structure numbers correspond to the same designs as in table 1

Table 2 : The specific on-resistance values extracted from simulation agree well with the values calculated using analytical models.

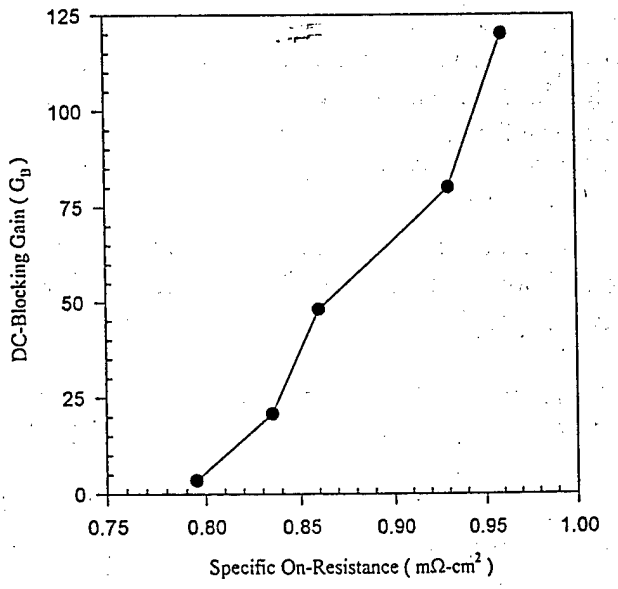

Fig. 15 : The trade-off between obtaining a high blocking gain at the cost of increased on-resistance.

In order to obtain a high blocking gain, it is necessary to pinch off the channel with a low gate bias. This can be done by using a small mesa-width, larger gate-length, lower doping or a Schottky gate with a higher contact potential. All of these result in a

higher specific on-resistance. The trade-off between obtaining a higher blocking gain at the cost of increased on-resistance is illustrated in figure 15.

E. Conclusions

It is evident from the above discussion that the U-MESFET is a suitable device to realize the potential of SiC as a superior replacement to silicon. It was seen that the structure with the lowest mesa-width (1 μm) has the best blocking gain (G_B = 120) and needs only 10 V gate bias to achieve the rated blocking voltage of 1200 V. However the on-resistance for this structure is the highest (9.6 x $10^{-4}\Omega$-cm^2). Also from a fabrication point of view, it is difficult to get mesa-widths of 1μm. The structure with 1.5 μm mesa-width needs 25 V gate bias to achieve the rated blocking voltage, a blocking gain of 48, and has a lower on-resistance (8.6 x 10^{-4} Ω-cm^2). While the on-resistance decreased for higher mesa-widths the blocking gain reduced rapidly and the structure with 3 μm mesa-width had a DC-blocking gain of only 3.5. **Thus the structure with mesa-width of 1.5 μm is the optimum design in terms of high blocking gain, low on-resistance and ease of fabrication.** Fabrication of the U-MESFET however involves filling at least 1.5 μm deep trenches with metal which is difficult, it is also difficult to obtain isolation between the gate and source metal which involves extremely critical alignments.

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[1] B. Jayant Baliga, "Trends in Power Semiconductor Devices," *IEEE Transactions on Electron Devices*, vol.43, No.10, pp.1717-1731, 1996.

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2. Fabrication of the HJFET

A. Introduction

As discussed in section III, the U-MESFET is an excellent device to realize the potential of silicon carbide as a replacement to silicon bipolar devices. However, the fabrication of a U-MESFET involves filling deep trenches with metal which is difficult. Further, for a metal gate, it is tough to obtain a good isolation between the gate and the source. In this section, a novel trench gate heterojunction field effect transistor (HJFET) (whose operation is identical to that of the U-MESFET) is analyzed. The process for fabricating the HJFET is presented. The HJFET shown in figure 1 has a P^+-polysilicon gate instead of the metal gate in the U-MESFET. Gate to source isolation is obtained by oxidizing the polysilicon before the source metallization. The fabrication of the HJFET involves a six mask level process with no critical alignments.

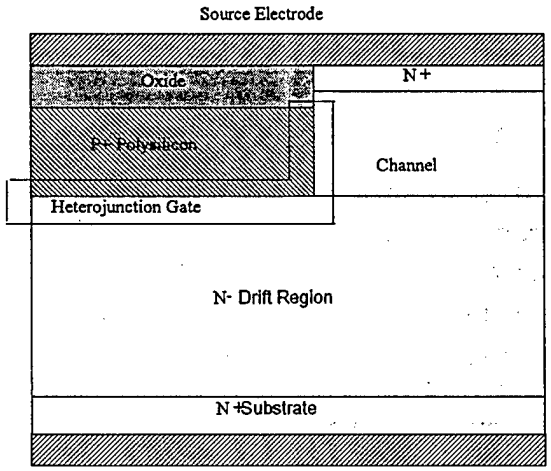


Fig. 1 : Cross-section of the HJFET, the polysilicon gate is oxidized to obtain isolation between the gate and source.

B. Process/Fabrication Sequence

The starting material for the fabrication of the HJFET was a [0001] oriented N^+ -SiC substrate (~300 μm thick) with an N-epitaxial layer (1×10^{16} cm^{-3}), with thickness of 10 μm. Two wafers , one of poly-type 4H and the other of poly-type 6H were used. The baseline process sequence is schematically illustrated in figure 2.

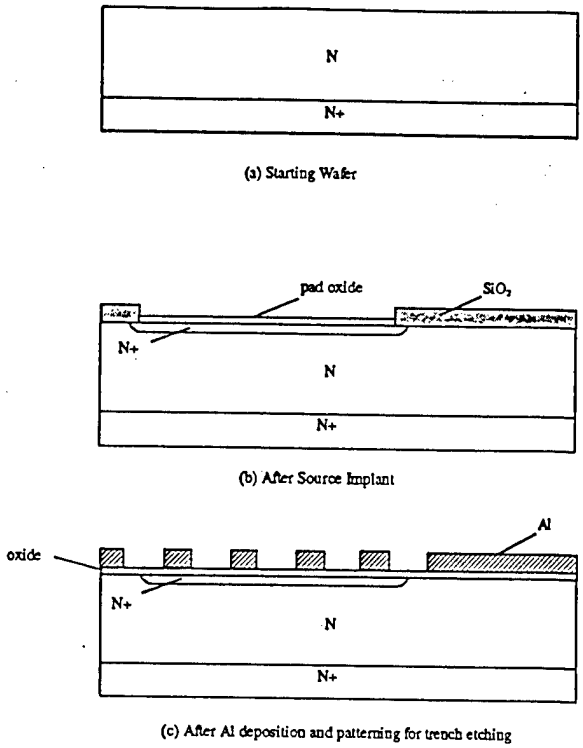


Fig. 2 : Process sequence of the HJFET

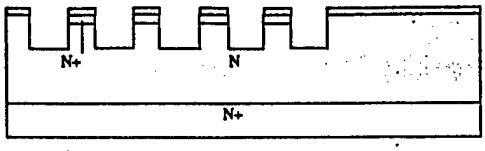
B.1 N^+ implant for the source contact

The first masking level was used for nitrogen implantation followed by high temperature annealing to obtain a shallow (~0.2 μm) N^+ region at the surface for the source contact. A 0.8 μm thick oxide layer was deposited by CVD and patterned by using a buffered oxide etch. A 0.2 μm thick pad oxide was then deposited by CVD. The nitrogen implantation and anneal were performed. The conditions were as follows :

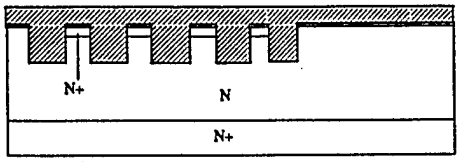
- Two successive implants with a dose of $1x10^{15}$ cm^{-2} and energies of 30 keV and 40 keV respectively.
- High temperature anneal was performed in a nitrogen ambient at 1250 °C for 30 min. to activate the dopants.

B.2 Removal of thick oxide

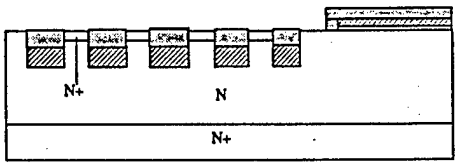
The second masking level was used to remove the entire oxide in areas outside the area with alignment marks and for certain devices designed with oxide under the source pad. A 0.2 μm thick oxide was deposited by CVD, to act as etch-stop during the poly etch back (described later).



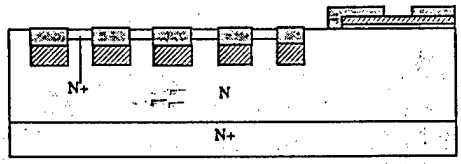
(d) After RIE and wet etch of Al mask



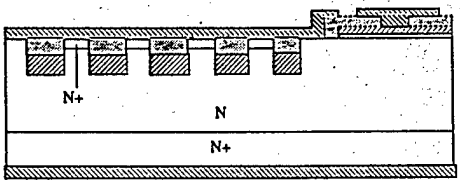
(e) After Poly Deposition



(f) After Poly etch-back & Oxidation



(f) After Contact etching



(g) After Final Al metallization and patterning

Fig. 2 : Process sequence of the HJFET (cont)

B.3 Trench etching and polysilicon refill

The third masking level was used to define the trench regions. Aluminum was used as the mask to etch trenches. The Al was patterned using lift-off lithography. 1.5 μm deep trenches were etched in SiC using RIE. The process used for RIE etches both SiC and oxide at the same rate and the 0.2 μm oxide was etched in the same step. The RIE was performed at the Microelectronics laboratory at NCSU and the conditions and the chemistry were as follows :

- Gases used, flow rates : SF_6 (9 sccm), O_2 (1 sccm).
- Chamber pressure : 50 mtorr
- Cathode temperature : 20 °C
- Power : 120 W
- The 1" SiC wafer was placed on the backside of a 4" Si wafer and a Teflon sheet with a 3" hole in the center was used to cover the aluminum cathode completely.
- The etch rate for SiC was ~ 150 A / s

It was found that the bottom surface of the trenches was rough, as shown in figure 3. This could cause the P^+-polysilicon / N-SiC heterojunction to have bad reverse I-V characteristics.

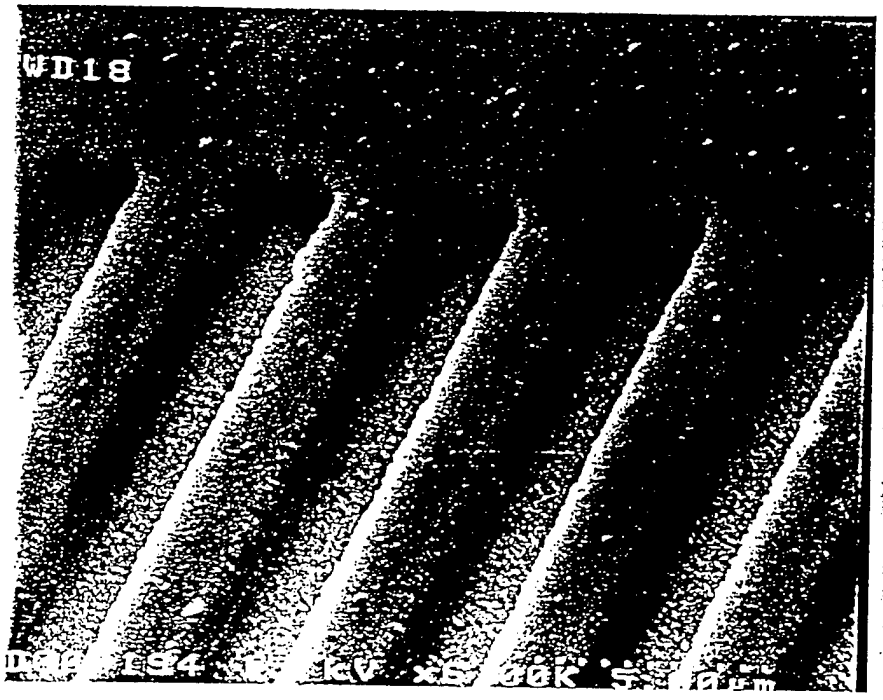


Fig.3: SEM micrograph of the wafer surface after trench-etching showing the roughness at the bottom of the trenches.

The Aluminum was then removed by wet chemical etching and 4 μm of undoped polysilicon was deposited to refill the trenches conformally. The polysilicon was then uniformly doped P-type by boron implantation and an anneal in nitrogen ambient to drive in the implant to get a uniform doping of approximately $1x10^{19}$ cm^{-3}. The polysilicon was deposited at Philips Research Laboratories, NY and the boron implant and anneal were done at MCNC. The conditions for the polysilicon deposition, the boron implantation and drive in were as follows:

- Polysilicon Deposition : 625 °C, SiH_4
- Boron implantation : Energy = 100 keV, dose = 2×10^{16} cm^{-2}
- Drive-in : 1250 °C for 4hr. in a nitrogen ambient.

B.4 Polysilicon etch back :

The fourth masking level was used to protect the polysilicon in the gate pad regions, before the polysilicon etch back for planarization. The polysilicon etch back was done using RIE at the microelectronics laboratory at NCSU. The etch rate for polysilicon was ~1750 A / s and the RIE was done for 27 min. to remove the entire polysilicon on the mesa regions. The conditions and chemistry for the RIE are as follows :

- Gases used, flowrates : SF_6 (15 sccm), O_2 (5 sccm)
- Chamber pressure : 60 mtorr
- Cathode temperature : 20 °C
- Power : 100 W

The polysilicon etch was non-uniform across the surface of the wafer, this would result in variation of the gate-lengths across the wafer surface.

In order to ensure that the mesa region of the silicon carbide does not get etched during this step, a 0.2 μm thick oxide was deposited by CVD prior to etching trenches. After the polysilicon etch back, the polysilicon in the trench was oxidized to obtain gate to source isolation. At this step, it is necessary to ensure that enough of the polysilicon inside the trench is oxidized such that there is no polysilicon in contact with the N^+-SiC in the mesa region, as this would result in gate to source shorts. Wet oxidation for 2.5 hours at 1000 °C was performed to oxidize the polysilicon. The oxidation rate for SiC is much lower than that for polysilicon and only 100 A.(approximately) of oxide was grown on the mesa region whereas there was about 8000 A of oxide grown in the trench region. The wafers were now subjected to an unmasked BOE (buffered oxide etch) dip for 40 s to etch the oxide on the mesa region, while retaining sufficient amount of oxide in the trench region to provide gate to source isolation.

B.5 Contact to the polysilicon gate

The fifth masking level was used to define the contact holes to the P^+- polysilicon gate pads. Photoresist was used as the mask and the wafers were subjected to a 13 minute BOE dip to etch away the oxide grown on the polysilicon (in the previous step) to open contact holes for the gate metal. At the end of the fourth step, polysilicon etch back and

oxidation, 4 μm thick polysilicon patterns for the gate pads were left. The photoresist spun on to the wafers could not cover the 4 μm step properly. Hence some of the oxide along the sidewalls of the polysilicon pads was etched during the contact hole etch. This could result in gate to source shorts, since the source metal runs over the sidewalls of the polysilicon pads as shown in figure 4.

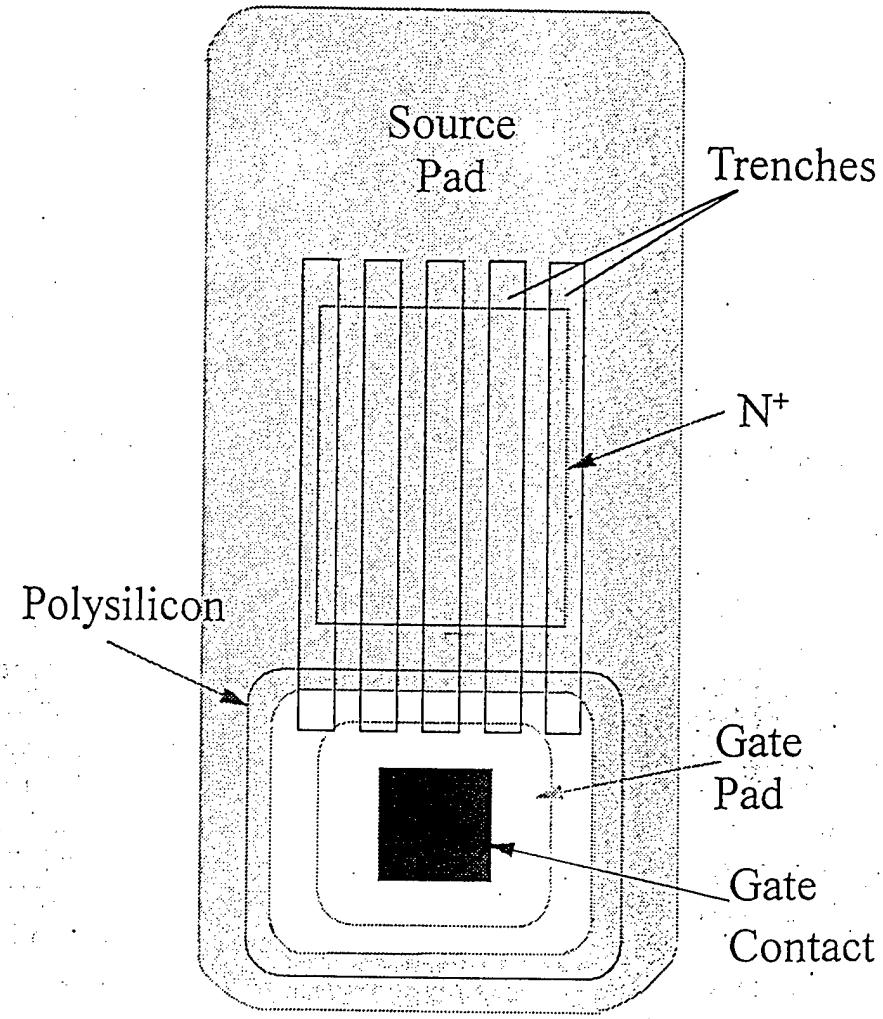


Fig. 4 : Mask Design for the HJFET. The source metal runs over the oxide on the polysilicon pad, if the oxide at the sidewall of the pad is etched during contact hole etching it would result in gate to source shorts.

B.6 Metallization

The sixth masking level was used to define the source and gate metal pads. The patterning was done by lift-off lithography. Negative photoresist was patterned on the wafer prior to the metallization. Both the front and backside metallizations involved sequential evaporation of 2000 A of Ti followed by 8000 A of Al.

B.7 Edge Termination

The edge termination for the P^+- polysilicon / N-SiC heterojunction was designed to be a Schottky contact followed by an argon ion implant to terminate the Schottky contact. The argon ion implantation has been shown to be an ideal termination technique for Schottky contacts [1]. As shown in the mask design in figure 4, the source metal (Ti) runs over the oxide on the polysilicon (grown in step 4) and forms a Schottky contact to the N-SiC surface.

C. Conclusions

The process for fabricating the HJFET is fairly simple and does not involve any critical alignments. The trench etching in SiC resulted in trenches with roughness at the bottom. This could cause the heterojunction gate to have a high leakage current. The polysilicon etch back was non-uniform and would result in variation of the gate-length from die to die across the wafer. The step coverage of the polysilicon pads by photoresist in the fifth masking level was poor and this could result in gate to source shorts. The polysilicon should be subjected to an unmasked etch prior to a masked etch so that the polysilicon pad is only about 1-1.5 μm thick in which case step coverage could be more easily achieved.

References:

[1] D. Alok, B. J. Baliga and P. K. McLarty, "A simple edge termination for silicon carbide devices with nearly ideal breakdown voltage," *IEEE Electron Device Lett.*, vol. 15, pp. 394-395, 1994.

3. Experimental Results, Conclusions and Future work

A. Introduction

In this section, the results of the experimental measurements on the HJFET fabricated on 4H-SiC are discussed. The conclusions from the fabrication and characterization of the HJFET are presented and suggestions for the future work are outlined.

B. Experimental Results

As discussed in section IV, in the fifth mask level of the HJFET process, the isolation oxide was etched away, due to bad photoresist step coverage of the polysilicon gate pads. This resulted in gate to source shorts. Hence, the triode-like blocking characteristics of the HJFET could not be experimentally observed. However, the HJFET showed current-saturation in the on-state due to channel pinch-off. Also the channel resistivity could be modulated at small gate-bias steps. The specific on-resistance of the HJFET was very low and close to the expected value.

B.1 On-Resistance

For the purposes of this analysis, the ideal specific on-resistance of the drift-region could be obtained using a $N^+/N^-/N^+$ test element fabricated in the HJFET process. The J-V curves of this test element and the different fabricated HJFET structures (at $V_{GS} = 0$ V) are shown in figure 1. The values of $R_{on,sp}$, calculated using the measured resistances are summarized in table 1. As expected the on-resistance of the HJFET decreases as the mesa-width (W_m) increases and the trench-width (W_t) decreases. The $N^+/N^-/N^+$ structure had an $R_{on,sp}$ of 1.74 mΩ-cm^2. The structure with W_m = 2 μm and trench-width (W_t)= 1 μm had the lowest $R_{on,sp}$ of 2.43 mΩ-cm^2 and is very close to the ideal value. The structure with W_m = 1 μm and W_t = 3 μm had an $R_{on,sp}$ of 9.68 mΩ-cm^2 which is about 9 times higher than the expected value. These values are 100 times better than values reported for SiC MOSFETs [1] demonstrating that the HJFET is a very promising structure for power switch development.

B.2 Forward-blocking :

The HJFET is a normally-on device and needs a negative potential between the gate and source in order to pinch-off the channel to provide forward blocking capability. However, due to the gate to source shorts, the device could not be turned-off. Inspite of this problem, it was found that the HJFET structures with narrow channel widths (W_m = 1 - 1.5 μm) exhibited current saturation in the on-state due to the channel being pinched-off by the drain bias. In addition despite the gate to source shorts, the channel resistivity could be modulated at small gate-biases (between -0.2 V to 0.2 V). The

figures 2-4. From these characteristics it can be observed that the structure with W_m = 1 μm saturates at a drain current of 0.01 A, which is much lower than the saturation current of 0.08 A for the structure with W_m = 1.5 μm.

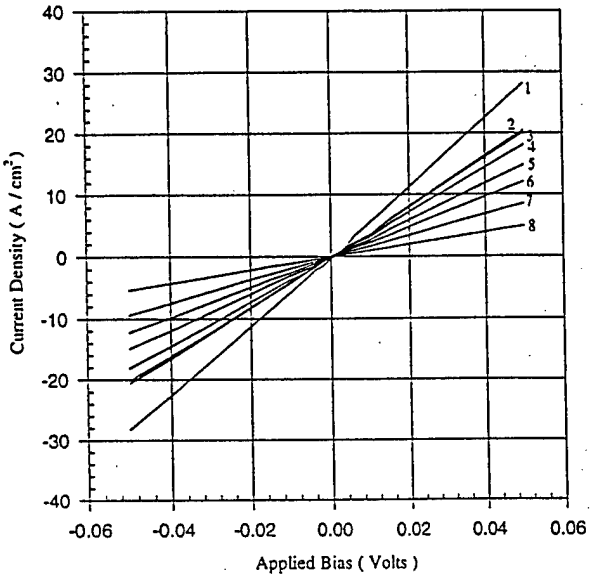


Fig. 1 : J-V characteristics to determine the $R_{on,sp}$ of the different HJFET structures

Curve (#)	mesa-width (W_m, μm)	trench-width (W_t, μm)	$R_{on,sp}$ (mΩ-cm^2)
1*	-	-	1.74
2	2	1	2.43
3	3	3	2.48
4	2.5	3	2.7
5	2	3	3.38
6	1.5	3	4.1
7	1	1	5.54
8	1	3	9.68

*This curve is for the N^+ / N^- / N^+ test element.

Table 1 : $R_{on,sp}$ of the different HJFET structure fabricated, the curve# corresponds to the curve in fig.1

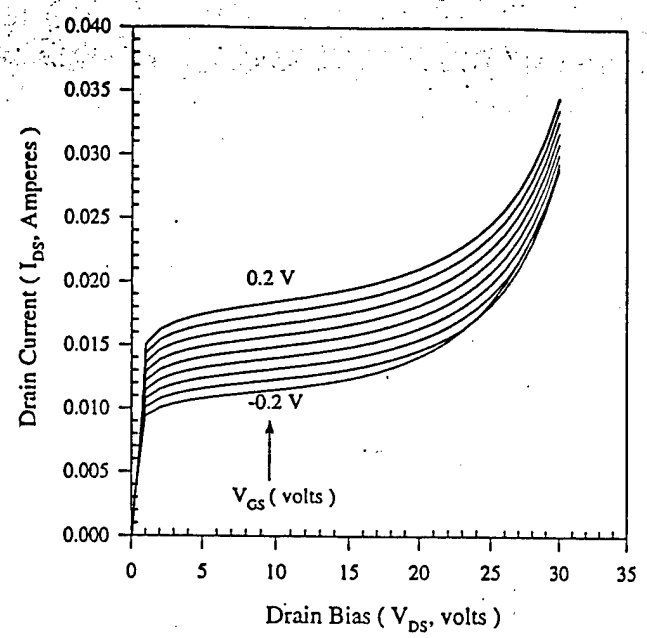


Fig. 2 : Pentode-like characteristics of the fabricated HJFET, $W_m = W_t = 1$ μm, the gate-bias is increased in steps of 50 mV.

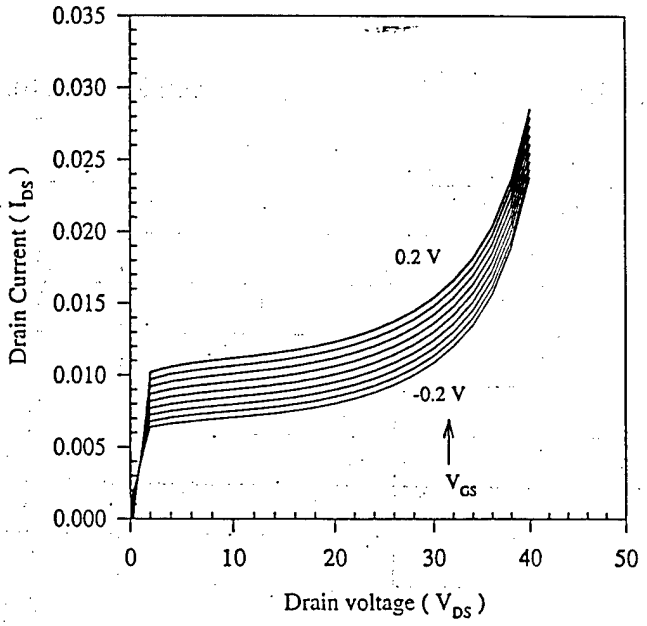


Fig. 3 : Pentode-like characteristics of the fabricated HJFET, $W_m = 1$, $W_t = 3$ μm, the gate-bias is increased in steps of 50 mV.

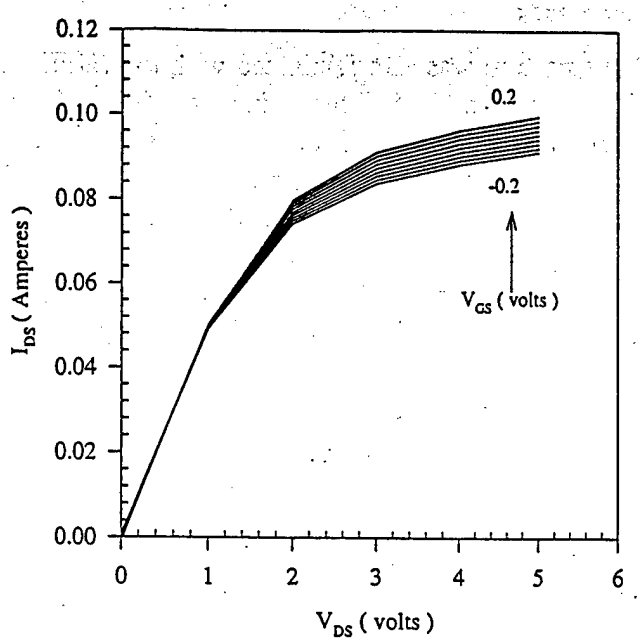


Fig. 4 : Pentode-like characteristics of the fabricated HJFET, W_m = 1.5, W_t = 3 μm, the gate-bias is increased in steps of 50 mV.

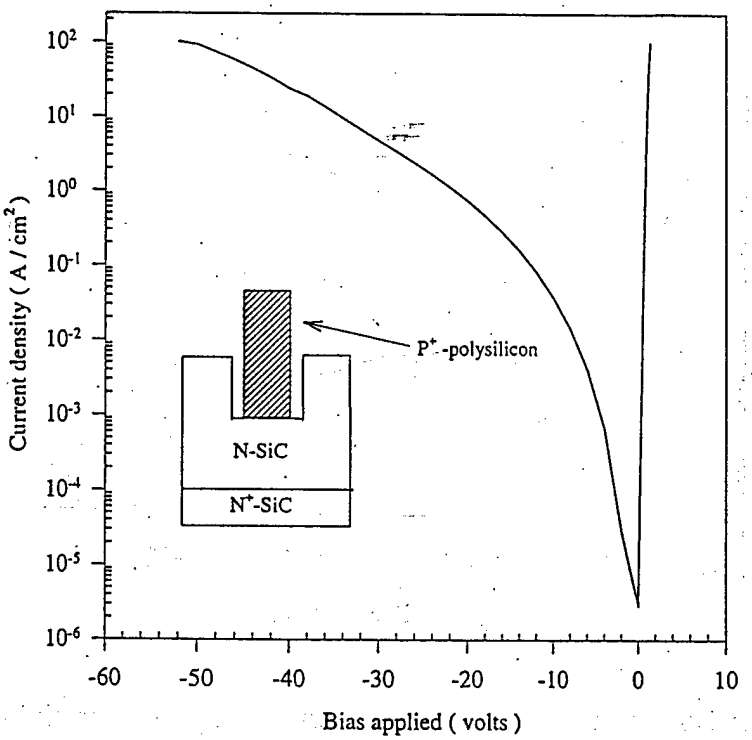


Fig. 5 : J-V characteristics of the heterojunction diode, the leakage currents are high due to the bad interface caused by the roughness at the trench bottom.

B.3 Measurements on test elements

A heterojunction diode structure was also fabricated with the HJFET structures to study the properties of the P^+-polysilicon / N-SiC heterojunction. The J-V characteristics of the heterojunction diode are shown in figure 5 demonstrating that the diode shows reasonably good rectification. However the leakage current density of the diode is quite high. This could be due to the roughness at the bottom of the trenches in SiC as described in section IV.

A Ti Schottky rectifier was also fabricated with the HJFET to verify the blocking capability of the material. This diode showed excellent J-V characteristics and blocked about 240 V in the reverse direction, which is the expected breakdown voltage for unterminated Schottky diodes[3]. The forward voltage drop for the diode was 0.8 V at 100 A / cm^2 The J-V characteristics of the Schottky rectifier are shown in figure 6.

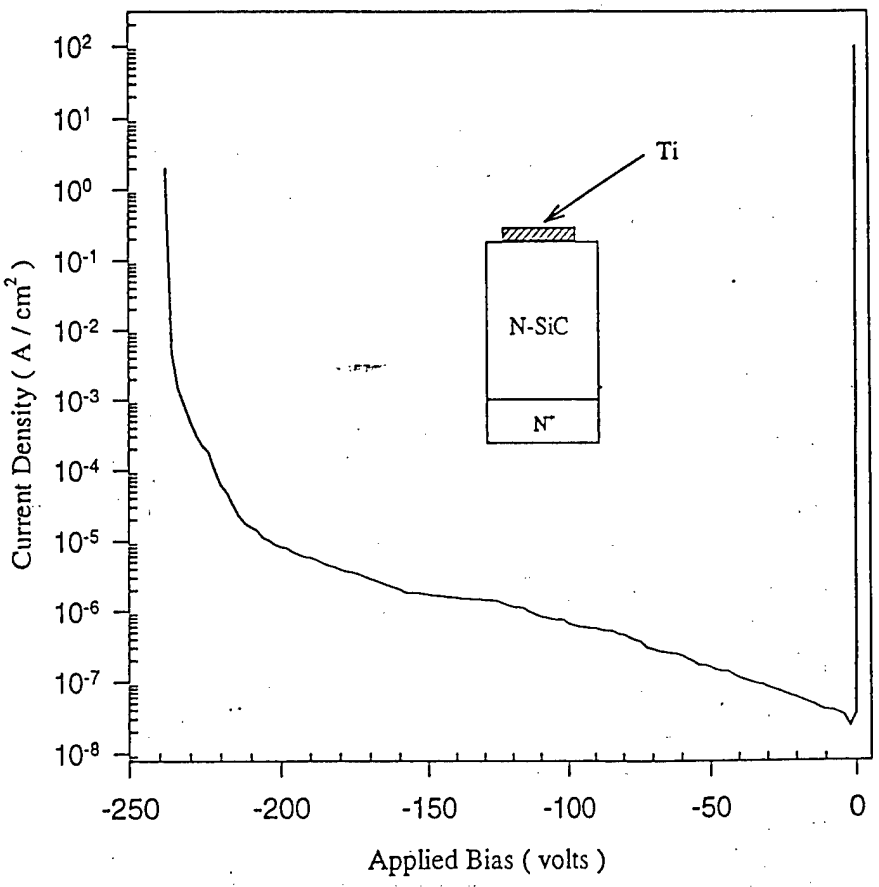


Fig. 6 : J-V characteristics of the Schottky diode test element. The breakdown for the unterminated structure is ~ 240 V

C. Conclusions and Future work

In conclusion, the simulations and experimental work performed in this research indicate that the HJFET is an excellent FET structure to utilize the advantages offered by SiC over silicon. The process for fabrication of the HJFET is fairly simple and does not involve any critical alignments. The operation of the HJFET depends on the ability of P^+-polysilicon /N-SiC heterojunction to block large voltages with a low leakage current. It is also important to be able to etch trenches with smooth side-walls and trench bottom.

However, the fabricated P^+-polysilicon / N-SiC heterojunction was found to have poor reverse I-V characteristics. The heterojunction was formed by depositing polysilicon in a trench etched in SiC. As discussed in section IV, the trenches etched in SiC were rough at the bottom. This results in a bad interface at the P^+-polysilicon / N-SiC junction giving rise to high leakage currents. It is important to standardize the RIE process for etching trenches in SiC so that trenches with smooth features can be obtained. The properties of the P^+-polysilicon / N-SiC heterojunction need to be carefully studied.

Poor step coverage by photoresist of the polysilicon pad at the fifth mask level resulted in gate to source shorts, severely hampering the performance of the HJFET. This problem could be avoided by subjecting the polysilicon to an unmasked etch, prior to a masked etch at the fourth mask level, so as to obtain a step of only 1 to1.5 μm, which could be easily covered, rather than a 4 μm step. Alternately, the sixth-mask level (for the metal patterning) could be redesigned such that the source metal does not run around the polysilicon pad thus, eliminating any possibility of gate to source shorts. However in this case an alternate edge termination would have to be designed for the polysilicon pad.

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A Planar Lateral Channel SiC Vertical High Power JFET

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Abstract: This paper describes a novel planar lateral channel SiC high power JFET structure. Two-dimensional numerical simulations predict low on-resistances with excellent current saturation and square FBSOA which have been experimentally confirmed. The fabricated 6H-SiC devices had a low specific on-resistance of 9 $m\Omega$-cm^2 at room temperature for a channel dose of $2x10^{13}$ cm^{-2}. This measured specific on-resistance is within 3X of the value calculated for the epitaxial drift region ($2.5x10^{16}$ cm^{-3}, 10μm). The 4H-SiC JFETs had excellent current saturation up to 1100V even at current densities as high as 250A/cm^2.

Introduction: Silicon carbide power MOSFETs with the UMOS structure have been recently reported [1-4]. These UMOSFETs suffer from two serious problems: (i) the high electric field at the trench corners causes destructive breakdown of the gate oxide at high drain voltages, and (ii) the extremely low inversion layer mobility [5] results in a higher specific on-resistance, nullifying the advantage of low drift region resistance in SiC. In the trench UMESFET structure [6], the low inversion layer mobility problem is eliminated, but this structure still suffers from the high electric fields at the sharp trench corners. Further, it requires a sophisticated process to achieve gate to source isolation in addition to high resolution lithography to allow channel pinch off with reasonable gate voltages. SiC lateral JFETs with buried gate contact have been reported by various groups [7-9]. These JFETs have low breakdown voltages (<100V) and have high specific on-resistances due to the lack of vertical current flow in these devices. Hence there is a need to consider alternate SiC FET structures. In this paper, we propose and demonstrate a new planar lateral channel, vertical SiC JFET structure with low on-resistance.

Device Structure and Simulations: The schematic cross-section of the proposed device is shown in Fig.1. A lateral channel is formed between the buried P^+ layer and the shallow P^+ surface gate. The thickness and doping of the channel region can be adjusted to create either a normally-on or -off device. The normally-on device is preferred as it will have a lower on-resistance. When a positive voltage is applied to the drain with the gate at zero bias, current flows from the drain through the gap in the buried P^+ layer and then through the channel to the source . The current flow can be modulated by applying a negative gate bias to deplete the channel region. If a sufficient negative bias is applied to the gate to pinch off the channel, a potential barrier is established for the flow of electrons from

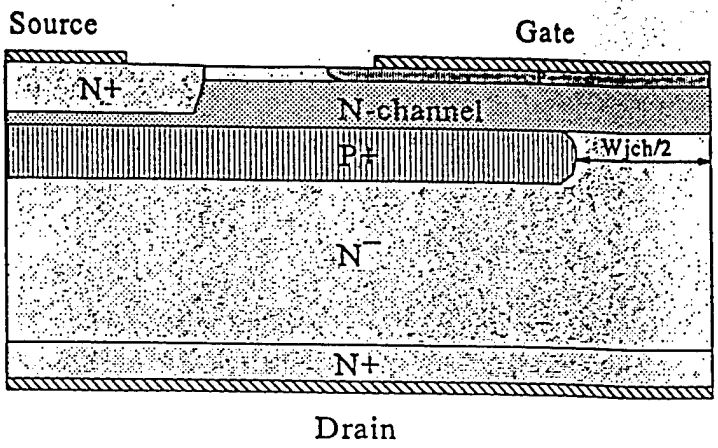

Fig.1 Schematic cross-section of the planar lateral channel SiC vertical JFET.

source to the drain. If the barrier is sufficient enough to stop the electron flow, then no current will flow even if the drain bias is increased until we reach the avalanche breakdown voltage. In order to prevent the drain potential from encroaching into the channel region and lowering the channel potential barrier, the channel has to be well shielded. This can be achieved by reducing the gap between the two P^+ layers (W_{Jch}) which also helps in reducing the electric field crowding at the P^+ layer edge thereby increasing the breakdown voltage of the device.

Two dimensional numerical simulations of the vertical JFET structure with a 10 μm thick 6H-SiC epitaxial layer with doping concentration of $2x10^{16}$ cm^{-3} were done using *MEDICI* [10]. Since the maximum energy chosen for the P-type boron implant was 400 KeV, the maximum channel thickness is only 0.35μm. This channel thickness is fully pinched off due to the built-in junction potentials if the channel doping is same as the epitaxial layer ($2x10^{16}$ cm^{-3}). In order to make a normally-on device, an N-type channel implant is required. Simulations were done with different N-channel implant doses

ranging from $1x10^{12}$ to $2x10^{13}$ cm^{-2}. The simulated current flow lines for such a device (N-channel dose=$2x10^{12}$ cm^{-2}) is shown in Fig.2. From the figure it can be seen that the current spreads rapidly in the drift region giving rise to a uniform current flow in the drift region, thus reducing the on-resistance. The current spreads much faster than a 45 degree angle due to the anisotropy of the mobility in 6H-SiC. In 6H-SiC, the lateral (perpendicular to the c-axis) mobility is about 5 times higher than the vertical mobility. This actually helps us in this device as the biggest contribution to the resistance comes from the channel which is lateral and therefore has 5 times less resistance.

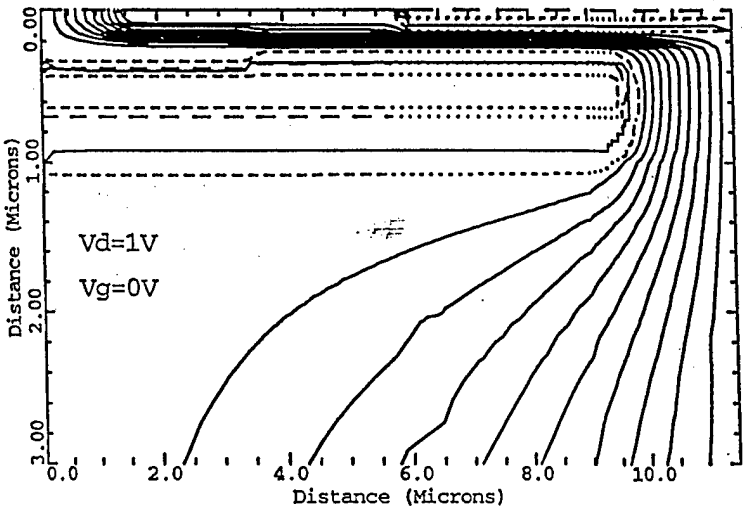

Fig.2 Simulated current flow lines in the planar 6H-SiC JFET at Vds=1V, Vgs=0V.

The simulated on-state and blocking characteristics are shown in Fig.3 and Fig.4 respectively. It may be noted that the device has low on-resistance and linear on-state characteristics even at high current densities due to the low channel resistance. It can be seen from Fig.5 that the potential contours are almost flat and that the field crowding at

the P^+ layer edge is minimal giving rise to near ideal breakdown voltage. From the blocking characteristics, it may be noted that the device has a high breakdown voltage of about 1025V and 960V for W_{Jch}=2 and 4μm respectively.

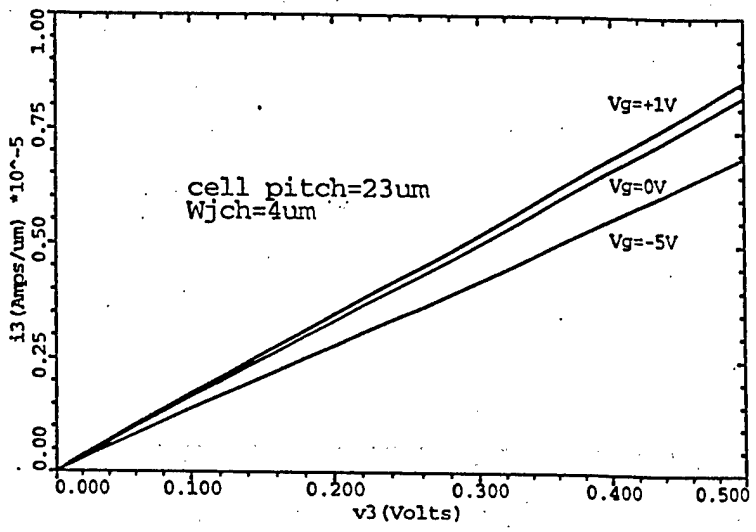

Fig.3 Simulated on-state I-V characteristics of the 6H-SiC JFET structure. (Dose=1e13/cm², Wjch=4 um)

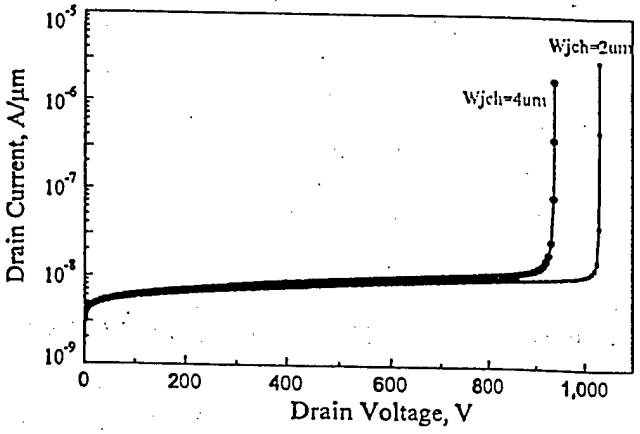

Fig.4 Simulated blocking characteristics of the planar 6H-SiC JFET structure.

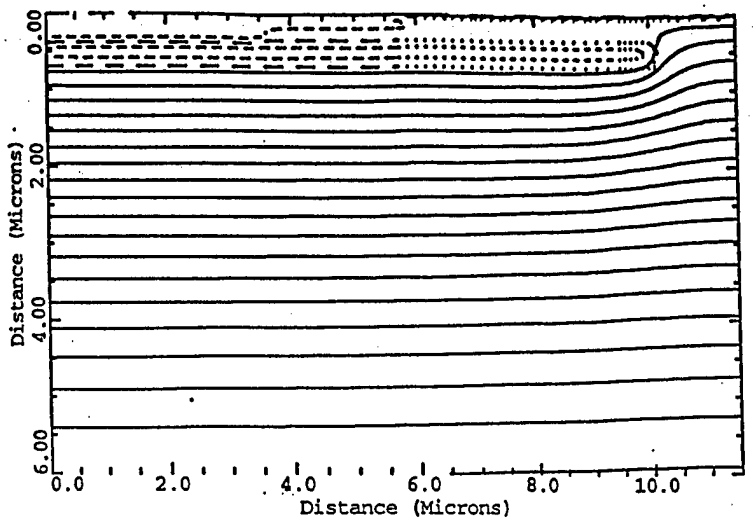

Fig.5 Simulated potential contours at a drain bias of 900V showing minimal electric field crowding at the buried junction edge in the planar 6H-SiC JFET structure.

As expected, the specific on-resistance ($R_{on,sp}$) decreased with increase in the dose as shown in Table.1 for 6H-SiC JFETs. A similar trend was observed for 4H-SiC devices also. The breakdown voltage remains almost constant for low values of channel doses but decreases as the channel dose is increased beyond $2x10^{12}$ cm^{-2}. For a given N-channel dose, the $R_{on,sp}$ also decreased with increase in the P^+ layer spacing (W_{Jch}) for both 6H- and 4H-SiC JFETs. However the breakdown voltage decreased slightly with increasing W_{Jch} due to higher electric field at the corner of the buried P^+ layer. Thus there is a trade-off between reducing the $R_{on,sp}$ and increasing the breakdown voltage by varying W_{Jch}.

W cell µm	W jch µm	Channel implant Dose /cm² x 10¹²	Ron,sp mOhm-cm²	BV Volts
23	4	1.0	28.7	957
23	4	1.4	19.1	955
23	4	2.0	13.8	948
23	4	10	7.0	901
21	2	1.0	28.9	1023
21	2	1.4	20.5	1022
21	2	2.0	15.4	1018
21	2	10	9.3	962

Table.1 Effect of N-channel dose and W jch on the 6H-SiC JFET parameters

Device Fabrication: The devices were fabricated on both 6H- and 4H-SiC with 10μm thick N-type homo-epitaxial layers grown on N^+ substrates. The epilayer doping concentration was $2.5x10^{16}$ cm^{-3} for 6H-SiC and $1.6x10^{16}$ cm^{-3} for 4H-SiC. A 9 mask process with 2μm design rule was used. The buried P^+ layer was formed by boron implantation at 380 KeV (dose=$1x10^{14}$ cm^{-2}) followed by multiple lower energy boron implants at the pad area so that contact could be made to the buried layer. A shallow 10 KeV boron implant (dose=$1x10^{15}$ cm^{-2}) was used to form the upper P^+ gate region. The N^+ source regions were formed by nitrogen implantation (40,100KeV, $8x10^{14}$ cm^{-2}). Three different N-channel doses of $1x10^{12}$, $1x10^{13}$ and $2x10^{13}$ cm^{-2} were used to study the effect of N-channel dose on the device characteristics. All implants were annealed at 1400 °C in argon for 30 minutes. Al ohmic contacts were made to the P^+ regions using RTA at 900 °C for 60 sec. Ti/Al was used for ohmic contacts to the N^+ source and drain regions.

Experimental Results: All the devices were characterized using a computerized Keithley model 251 system at room temperature. All the JFETs except those which received 10^{12} cm^{-2} dose N-channel implant exhibited pentode-like characteristics with excellent on-resistance and good saturation characteristics. The devices with $1x10^{12}$ cm^{-2} dose N-channel implant were normally-off and had very high on-resistance due to the absence of a conducting channel. The on-state performance of these devices could not be improved even by applying a positive gate bias since the maximum positive gate bias was limited to about 3V, beyond which the gate current increases rapidly. Hence only the results obtained on the $1x10^{13}$ and $2x10^{13}$ cm^{-2} dose devices are reported below. Since the devices on 6H-SiC and 4H-SiC had different characteristics, they are discussed separately.

6H-SiC JFETs: The on-state I-V characteristics of two typical 6H-SiC devices which received the different doses of N-channel implants are shown in Fig.6 (a) and (b). It can be seen that the devices are normally-on with very good conduction at zero gate bias. They had excellent specific on-resistance of 11 $m\Omega\text{-}cm^2$ for channel dose of $1x10^{13}$ cm^{-2} and 9 $m\Omega\text{-}cm^2$ for channel dose of $2x10^{13}$ cm^{-2}. These measured values come close to the specific on-resistances obtained from simulation of 7 $m\Omega\text{-}cm^2$ for a dose of $1x10^{13}$ cm^{-2} and 6.3 $m\Omega\text{-}cm^2$ for $2x10^{13}$ cm^{-2} . It is worth pointing that the ideal $R_{on,sp}$ is 3.2 $m\Omega\text{-}cm^2$ (for 10μm, $2.5x10^{16}$ cm^{-3} doped epilayer) and hence these fabricated devices have specific on-resistances within 3X of the ideal value. The gate bias could modulate the drain current well by pinching off the channel for the devices which received a channel dose of $1x10^{13}$ cm^{-2}. However, the gate bias had only little control over the drain current on those which received a channel dose of $2x10^{13}$ cm^{-2} due to the higher channel doping.

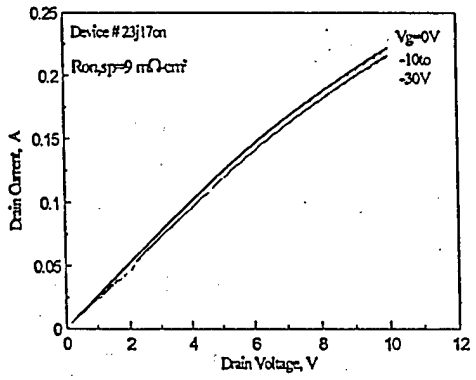

Fig.6 (b) Measured on-state I-V characteristics of the 6H-SiC JFET (dose=2e13/cm²)

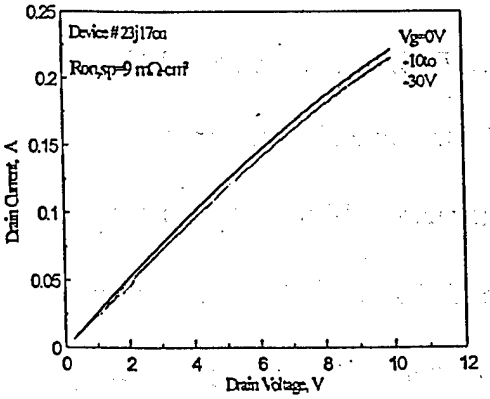

Fig.6 (b) Measured on-state I-V characteristics of the 6H-SiC JFET (dose=2e13/cm²)

The output characteristics of the $1x10^{13}$ and $2x10^{13}$ cm^{-2} dose devices are shown in Fig.7 (a) and (b). The devices had low on-resistance followed by excellent saturation as predicted by simulations. It may be pointed out that though the devices with lower channel doping showed better gate control, they could not be taken to the blocking mode because the gate to source junction breaks down at about -60V due to the high channel doping.

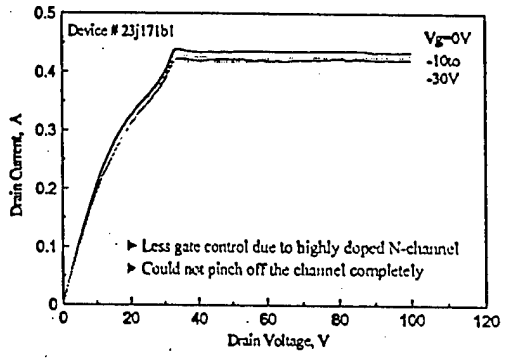

Fig.7 (b) Measured output characteristics of the 6H-SiC JFET (dose=2e13/cm²)

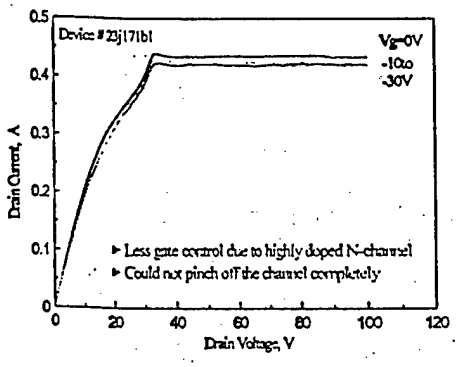

Fig.7 (b) Measured output characteristics of the 6H-SiC JFET (dose=2e13/cm²)

4H-SiC JFETs: The on-state I-V characteristics of two typical 4H-SiC devices which received the two different implants are shown in Fig.8 (a) and (b). They had low specific on-resistance of 14 $m\Omega$-cm^2 for channel dose of $1x10^{13}$ cm^{-2} and 11 $m\Omega$-cm^2 for channel dose of $2x10^{13}$ cm^{-2}. Calculations show that the ideal $R_{on,sp}$ is 0.42 $m\Omega$-cm^2 (for 10μm, $1.6x10^{16}$ cm^{-3} doped epilayer) and hence the specific on-resistance of the fabricated devices is much higher (~30X) than the ideal value. The 4H-SiC JFETs exhibited better gate control for both N-channel implant doses when compared with the 6H-SiC devices.

Figures 9 (a) & (b) shows the output characteristics of both the $1x10^{13}$ and $2x10^{13}$ cm^{-2} dose devices. The devices had low on-resistance followed by excellent current

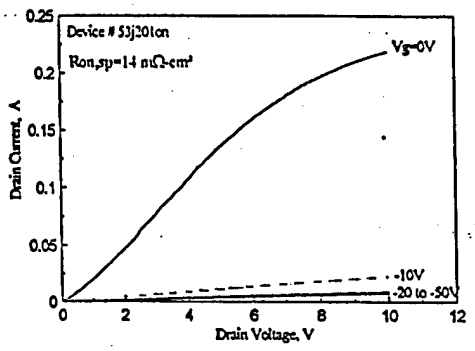

Fig.8 (a) Measured on-state I-V characteristics of the 4H-SiC JFET (dose=1e13/cm²)

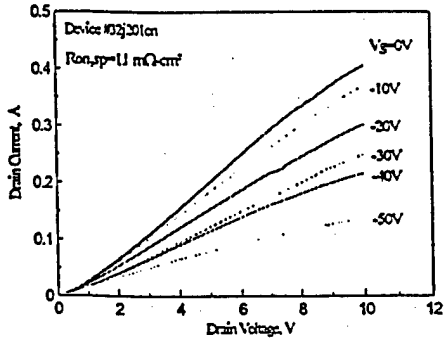

Fig.8 (b) Measured on-state I-V characteristics of the 4H-SiC JFET (dose=2e13/cm²)

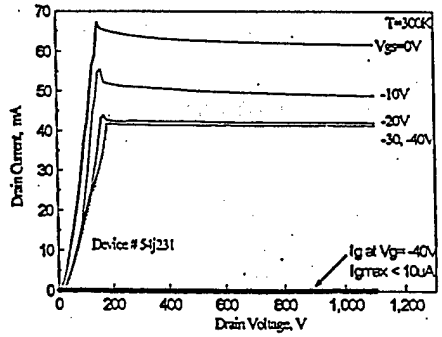

Fig.9 (a). Measured output characteristics of the JFET fabricated on 4H-SiC showing excellent current saturation with BV>1100V.

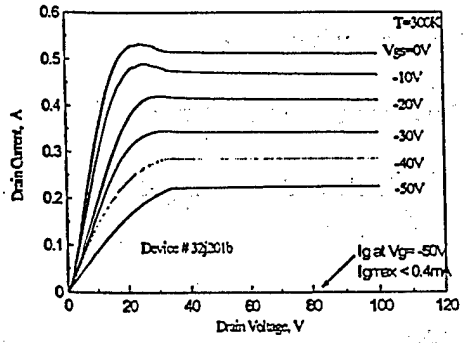

Fig.9 (b) Measured output characteristics of the 4H-SiC JFET (dose=2e13/cm²)

saturation characteristics. For one device which received a channel dose of $1x10^{13}$ cm^{-2}, the saturation current was below 100mA (the maximum limit on the high voltage measurement equipment) and therefore the drain voltage could be increased up to 1100V. It can be seen from the output characteristics (Fig.9(a)) that the device had excellent saturation up to 1100V indicating a wide FBSOA. It may be pointed out that though the devices had the expected characteristics with good gate control, they could not be taken

to the blocking mode because the gate to source junction breaks down at about 50-60V due to the high channel doping.

Conclusions: Planar high voltage lateral channel vertical SiC JFET devices with low specific on-resistances (within 3X of ideal) were proposed and experimentally demonstrated. It may be pointed out that the on-resistance decreased with increasing N-channel dose for both 6H- and 4H-SiC. Excellent current saturation up to 1100V was measured at current densities as high as 250A/cm^2 on 4H-SiC JFETs. These devices may be of interest as high voltage current limiters. Even though the devices had good on-state and saturation characteristics, they could not be completely pinched off due to premature breakdown of the gate junction at about 50V. By comparing the characteristics of the devices with the different doses, it is evident that the lowest dose device had poor on-state characteristics whereas the higher dose devices had poor blocking characteristics. Hence a dose lower than 10^{13} cm^{-2} but higher than 10^{12} cm^{-2} should give us the best compromise between on-state and blocking characteristics.

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The Planar Lateral Channel MESFET- A New SiC Vertical Power Device

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Abstract: A novel planar lateral channel SiC MESFET structure with vertical current flow in the drift region is proposed and demonstrated by modeling and fabrication. The normally-on devices fabricated with high channel implant doses had a low room temperature specific on-resistance of 13 $m\Omega\text{-}cm^2$ and 11.2 $m\Omega\text{-}cm^2$ for 6H-SiC and 4H-SiC MESFETs, respectively but poor breakdown voltage (~15V). The normally-off devices fabricated with low channel doses had high breakdown voltage (~500V), but poor on-state resistance.

Introduction: The specific on-resistance of silicon carbide power FETs have been projected to be far superior to their silicon counterparts due to the high breakdown field strength of SiC [1]. Most of the research on silicon carbide power switches has been focused on the UMOSFET structure due to the inability to form diffused junctions in SiC. These UMOSFETs suffer from two serious problems: (i) the high electric field at the trench corners causes destructive breakdown of the gate oxide at high drain voltages, [2] and (ii) the extremely low inversion layer mobility [3] results in a higher specific on-resistance, nullifying the advantage of low drift region resistance in SiC. Recently, high voltage 4H-SiC UMOSFETs were reported [4] which can block up to 1100V (<40% of ideal BV_{pp}). However, due to low inversion channel mobility (1.5 $cm^2/V.s$), these devices had very high specific on-resistance of 433 $m\Omega\text{-}cm^2$ (at 300K) which is 125 times higher than the ideal calculated epilayer specific on-resistance. The problems of high electric field in the gate oxide and the low channel (inversion layer) mobility have not been fully addressed in this device. A device that eliminates the low inversion layer mobility problem is the trench UMESFET structure, [5] but this structure still suffers from the high electric fields at the sharp trench corners. Further, it requires a sophisticated process to achieve gate to source isolation in addition to high resolution lithography to allow channel pinch off with reasonable gate voltages. Hence there is a need to create alternate SiC FET structures. In this paper, we propose and demonstrate a new planar lateral channel, vertical SiC MESFET structure.

Device Structure and Simulations: The schematic cross-section of the proposed device is shown in Fig.1. A lateral channel is formed between the buried P^+ layer and Schottky gate on the top surface. The thickness and doping of the channel region can be adjusted to

create either a normally-on or -off device. The normally-on device is preferred as it will have a lower on-resistance. When a positive voltage is applied to the drain with the gate at zero bias, current flows from the drain through the gap in the buried P^+ layer and then through the channel to the source. The current flow can be modulated by applying a negative gate bias to deplete the channel region. If a sufficient negative bias is applied to the gate to pinch off the channel, a potential barrier is established for the flow of electrons from source to the drain. If the barrier is sufficient enough to stop the electron flow, then no current will flow even if the drain bias is increased until we reach the avalanche breakdown voltage. In order to prevent the drain potential from encroaching in to the channel region and lowering the channel potential barrier, the channel has to be well shielded. This can be achieved by reducing the gap between the two P^+ layers (W_{Jch}) which also helps in reducing the electric field crowding at the P^+ layer edge thereby increasing the breakdown voltage of the device.

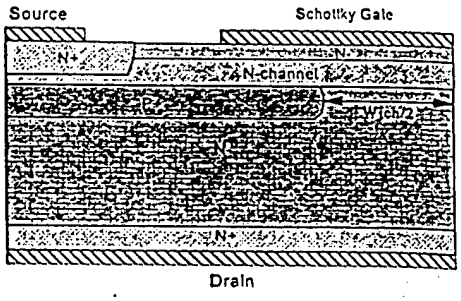

Fig.1 Schematic cross-section of the lateral channel vertical MESFET.

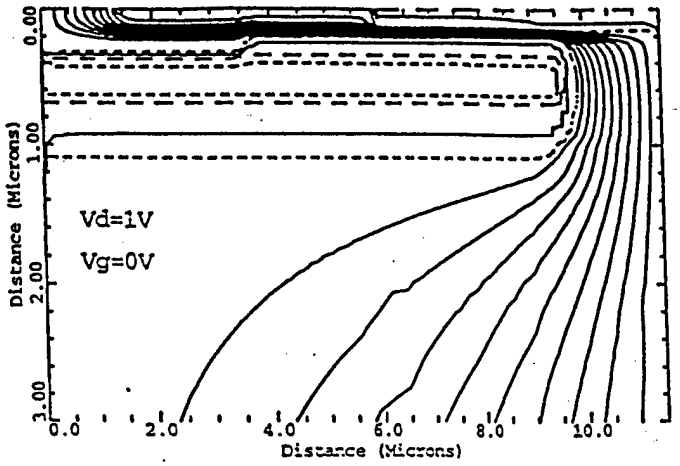

Fig.2 On-state current flow lines in the 6H-SiC MESFET structure. Vg=0V, Vd=1V.

Two dimensional numerical simulations of the vertical MESFET structure with a 10 μm thick 6H-SiC epitaxial layer (N_D=2x10^{16} cm^{-3}) were done using *MEDICI*. Since the maximum energy chosen for the P-type boron implant was 400 KeV, the maximum channel thickness is only 0.35μm. This channel thickness is fully pinched off due to the built-in junction potentials if the channel doping is the same as the epitaxial layer (2x10^{16} cm^{-3}). In order to make a normally-on device, an N-type channel implant is required. Simulations were done with different N-channel implant doses ranging from 1x10^{12} to 2x10^{13} cm^{-2}. The simulated current flow lines for such a device (dose = 2x10^{12} cm^{-2}) are shown in Fig.2. From the figure, it can be seen that the current spreads rapidly in the drift region giving rise to a uniform current flow in the drift region, thus reducing the on-resistance. The current spreads much faster than the usual 45 degree angle due to the anisotropy of the mobility in 6H-SiC. In 6H-SiC, the lateral (perpendicular to the c-axis) mobility is about 5 times higher than the vertical mobility. This actually helps us in this device as the biggest contribution to the resistance comes from the channel which is lateral and therefore has 5 times less resistance.

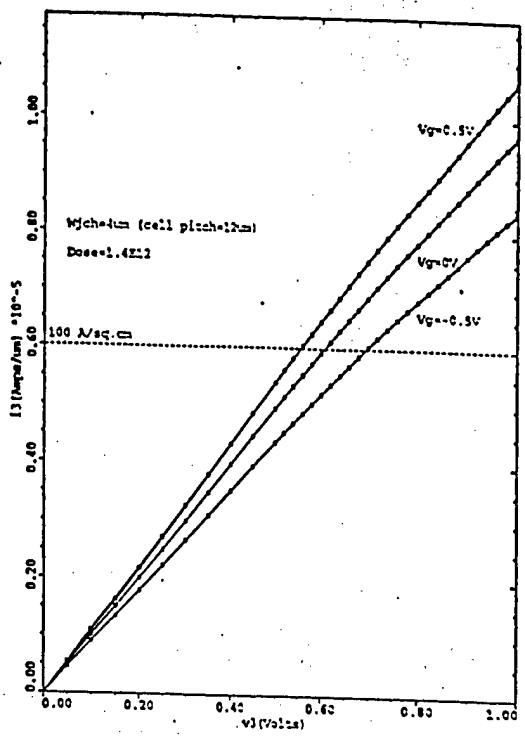

Fig.3 Simulated on-state I-V characteristics of the 6H-SiC MESFET structure. (Dose=1.4e12/cm² , Wjch= 4um)

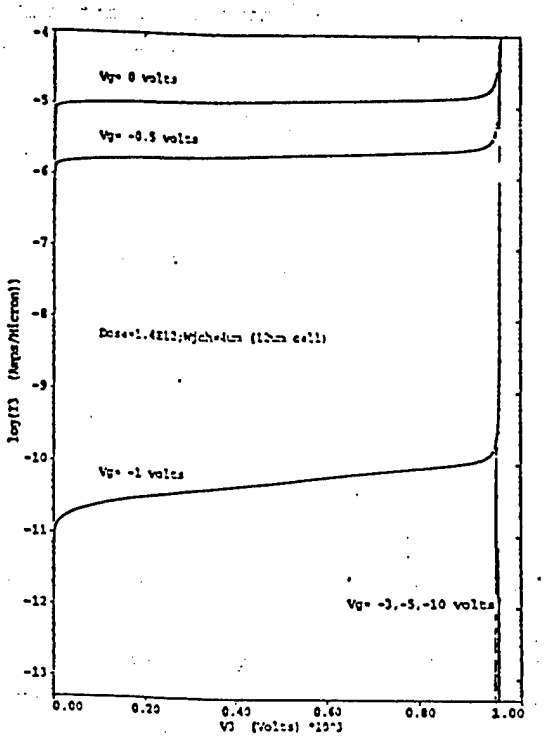

Fig.4 Simulated output characteristics of the 6H-SiC MESFET structure. (Dose=1.4e12/cm² , Wjch= 4um)

The simulated on-state and output characteristics are shown in Fig.3 and Fig.4 respectively. It may be noted that the device has low on-resistance and linear on-state characteristics even at high current densities due to the low channel resistance. From the output characteristics, it may be noted that the device has a high breakdown voltage of about 955V and a square FBSOA which is highly desirable for a power device.

Wcell μm	Wjch μm	Channel Implant Dose /cm²	Ron,sp mOhm-cm²	BV Volts
23	4	1E12	23.9	957
23	4	1.4E12	16.3	955
23	4	2E12	12.5	948
23	4	1E13	6.8	901
21	2	1E12	24.0	1023
21	2	1.4E12	17.6	1022
21	2	2E12	14.1	1018
21	2	1E13	9.0	962

Table.1 Effect of N-channel dose and Wjch on the 6H-SiC MESFET parameters

As expected, the specific on-resistance ($R_{on,sp}$) decreased with increase in the channel implant dose as shown in Table.1 for 6H-SiC MESFETs. Due to higher electron mobility, 4H-SiC devices had lower (≈3X) specific on-resistance than their 6H-SiC counterparts (4mΩ-cm^2 versus 12.5mΩ-cm^2 for a channel dose of 2x10^{12} cm^{-2}). As the channel dose is increased, the gate voltage required to pinch off the channel also increases, for example - a -10V bias is sufficient for a 2x10^{12} cm^{-2} dose whereas a -50V gate bias is required when the dose is at 2x10^{13} cm^{-2}. The breakdown voltage remains almost constant for low values of channel doses but decreases as the channel dose is increased beyond 2x10^{12} cm^{-2}. For a given N-channel dose, the $R_{on,sp}$ also decreased with increase in the P$^+$ layer spacing (W_{Jch}) for both 6H- and 4H-SiC devices. However the breakdown voltage decreased slightly with increasing W_{Jch} due to higher electric field at the corner of the buried P$^+$ layer. The simulated devices had good blocking characteristics with a breakdown voltage of about 1020V and 955V for W_{Jch}=2 and 4μm, respectively.

Thus, there is a trade-off between reducing the specific on-resistance and increasing the breakdown voltage by varying W_{Jch}.

Device Fabrication: The devices were fabricated on both 6H- and 4H-SiC with 10μm thick N-type homo-epitaxial layers grown on N^+ substrates. The epilayer doping concentration was $2.5x10^{16}$ cm^{-3} for 6H-SiC and $1.6x10^{16}$ cm^{-3} for 4H-SiC. An 8 mask process with 2μm design rule was used. The buried P^+ layer was formed by boron implantation at 380 KeV followed by multiple lower energy boron implants at the pad area so that contact could be made to the buried layer. The N^+ source regions were formed by nitrogen implantation (dose=$1.6x10^{15}$ cm^{-2}). Different N-channel doses in the range of $1x10^{12}$ to $2x10^{13}$ cm^{-2} were used to study the effect of N-channel dose on the device characteristics. All implants were annealed at 1400 °C in argon for 30 minutes. Al ohmic contacts were made to the P^+ regions using RTA at 900 °C for 60 sec. Ti/Al was used for ohmic contacts to the N^+ source and drain regions and simultaneously to form the Schottky gate contacts to the N^- regions to reduce process complexity.

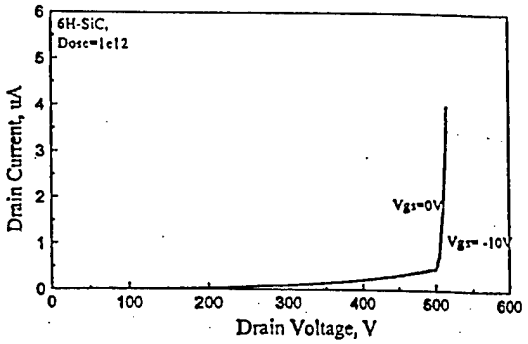

Fig.5 Output characteristics of a typical 6H-SiC MESFET with N-channel dose of 1e12/cm².

Experimental Results: All the devices were characterized using a Keithley model 251 system at room temperature. The devices with less than $2x10^{12}$ cm^{-2} dose N-channel implant were normally-off as shown in Fig.5 and had very high on-resistance at zero gate bias due to the absence of a conducting channel. The on-state performance of these devices could not be improved even by applying a positive gate bias since the maximum positive gate bias was limited to about 2V, beyond which the gate current increased rapidly. However, the devices with high N-channel doses beyond $1x10^{13}$ cm^{-2} had good on-state conduction characteristics. Hence only the results obtained on the $1x10^{13}$ and $2x10^{13}$ cm^{-2} dose devices are reported below. Since the devices on 6H-SiC and 4H-SiC had different characteristics, they are discussed separately.

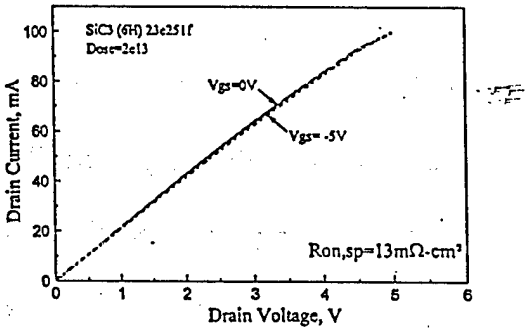

Fig.6 (b) Measured on-state I-V characteristics of the 6H-SiC MESFET (dose=2e13/cm²)

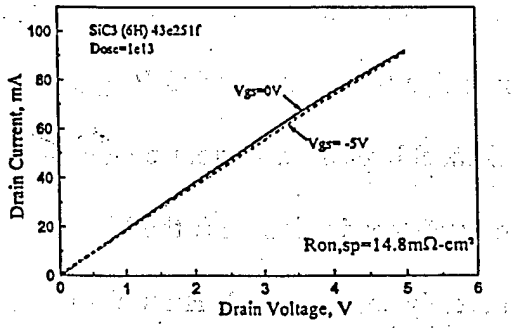

Fig.6 (a) Measured on-state I-V characteristics of the 6H-SiC MESFET (dose=1e13/cm²)

6H-SiC MESFETs: Figures 6 (a) and (b) show the on-state I-V characteristics of typical 6H-SiC devices fabricated using channel implant doses of $1x10^{13}$ and $2x10^{13}$ cm^{-2}. It can be seen that the devices are normally-on with very good conduction at zero gate bias. They had excellent specific on-resistance of 14.8 $m\Omega$-cm^2 for channel dose of $1x10^{13}$ cm^{-2} and 13 $m\Omega$-cm^2 for channel dose of $2x10^{13}$ cm^{-2}. It is worth pointing that the ideal $R_{on,sp}$ is

3.2 $m\Omega\text{-}cm^2$ (for 10μm, $2.5x10^{16}$ cm^{-3} doped epilayer) and hence the specific on-resistance of the fabricated devices is only 4X higher than the ideal value. The measured specific on-resistance is higher than the ideal value due to the contributions from the channel, JFET and substrate resistances, of which the channel is the most significant and can be reduced by increasing the channel dose. It may be noted that the on-resistance decreased with increasing N-channel dose as expected. However, it was observed that the gate bias had only little effect on the drain current for these devices fabricated with high channel dose and these devices could not be taken to the blocking mode. It was found that the gate contact was very leaky under reverse bias, as shown in Fig.7, which made it impossible to pinch off the channel. We believe that the high dose channel implants increased the surface concentration at the Schottky interface resulting in high reverse leakage currents for the Schottky junction. Attempts to pinch off the channel by applying negative bias to the buried P^+ gate were unsuccessful due to the metal gate acting as a channel bypass for current conduction. Thus even though, we were able to get excellent on-state conduction with the higher doses as expected, the blocking characteristics were severely compromised. High channel doses are required to get good on-state conduction, however this results in increasing the surface concentration at the Schottky gate contact leading to a leaky gate. The gate leakage current can be reduced by using a high barrier (>1eV) Schottky contact metal to form the gate contact. This will result in increased process complexity as a multiple metal process may have to be used to achieve this.

4H-SiC MESFETs: The on-state I-V characteristics of two typical 4H-SiC devices fabricated with two channel implant doses are shown in Fig.8 (a) and (b). It can be seen

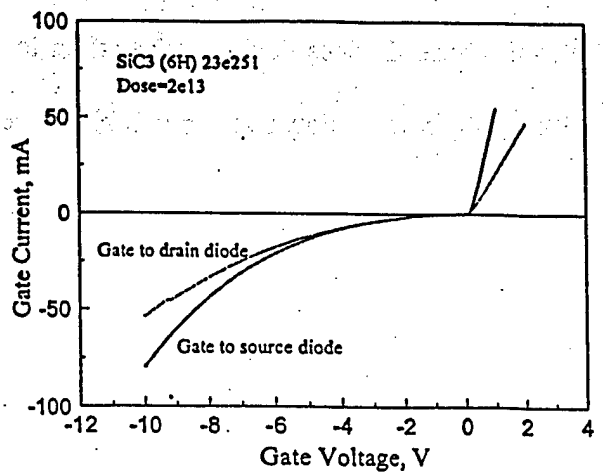

Fig.7 The I-V characteristics of typical Gate to Source and Gate to Drain diodes on 6H-SiC devices.

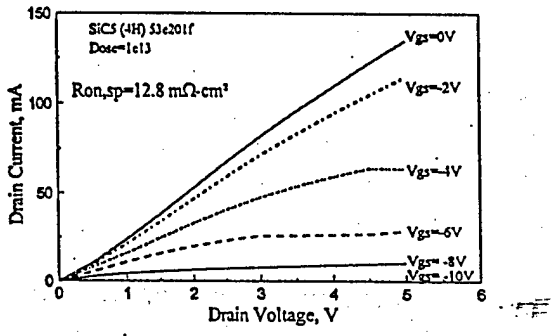

Fig.8 (a) Measured on-state I-V characteristics of the 4H-SiC MESFET (dose=1e13/cm²)

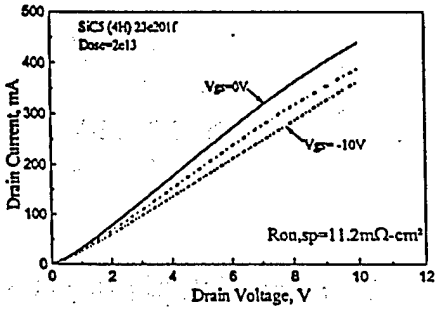

Fig.8 (b) Measured on-state I-V characteristics of the 4H-SiC MESFET (dose=2e13/cm²)

that both the devices are normally-on with good conduction at zero gate bias. They had low specific on-resistance of 12.8 mΩ-cm^2 for the channel dose of 1x10^{13} cm^{-2} and 11.2 mΩ-cm^2 for the channel dose of 2x10^{13} cm^{-2}. Calculations show that the ideal $R_{on,sp}$ is 0.42 mΩ-cm^2 (for 10μm, 1.6x10^{16} cm^{-3} doped epilayer) and hence the specific on-resistance of the fabricated devices is much higher (~30X) than the ideal value. Good gate control was observed on the devices fabricated with channel dose of 1x10^{13} cm^{-2} as shown in Fig.8(a). However, these devices could block only 15V due to the breakdown of the Schottky diode between gate and drain at about 25V as shown in Fig.9. For the devices which had the higher (2x10^{13} cm^{-2}) dose implant, the gate had little control over the drain current due

to the higher channel concentration. These devices could not be taken to the blocking mode of operation as the Schottky gate breaks down at around 20V, even before the channel could be pinched off.

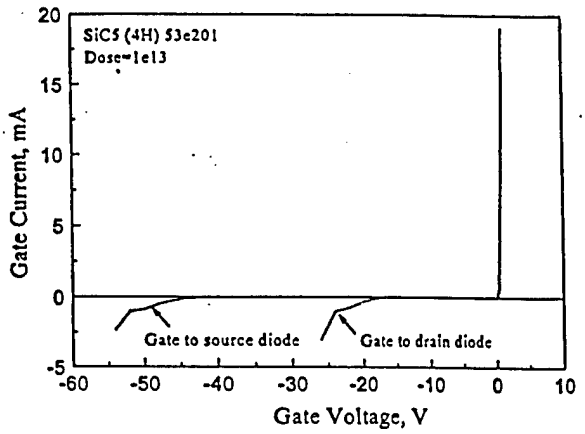

Fig.9 The I-V characteristics of typical Gate to Source and Gate to Drain diodes on 4H-SiC MESFETs.

Conclusions: Planar lateral channel SiC MESFETs with low specific on-resistances were proposed and experimentally demonstrated. The on-resistance decreased with increasing N-channel dose for both 6H- and 4H-SiC devices. Even though increasing the channel dose improved the on-state characteristics, the blocking voltage reduced significantly. This shows that the channel has to be optimized very carefully to obtain good forward conduction and blocking characteristics. Gate controlled current saturation was observed on 4H-SiC MESFETs with $1x10^{13}$ cm^{-2} dose channel implant, though the device had low blocking voltage. The high channel dose devices on both 6H- and 4H-SiC wafers had good on-state characteristics, but they could not be turned off due to the leaky Schottky gate junction. By comparing the characteristics of the devices with the different doses, it is evident that the low dose devices have poor on-state characteristics but good blocking characteristics whereas the higher dose devices had excellent on-state drops but poor

blocking characteristics. This shows that the value of N-channel dose is critical and a dose between 10^{12} and 10^{13} cm^{-2} is required to give the best compromise between on-state and blocking characteristics.

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Analysis and Optimization of the Planar 6H-SiC ACCUFET

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Abstract: This paper discusses the optimization of the planar 6H-SiC ACCUFET structure based upon analysis, simulations and experimental results. Two-dimensional numerical simulations demonstrate that the maximum electric field in the gate oxide can be kept below 3.5MV/cm even at the maximum blocking voltage of 1500V, by proper device design thereby eliminating the oxide rupture problem seen in SiC UMOSFETs. The trade-off between specific on-resistance and the maximum gate oxide electric field is obtained using simulations. The fabricated 6H-SiC unterminated devices had a blocking voltage of about 350V with a specific on-resistance of 18 $m\Omega$-cm^2 at room temperature for a gate bias of only 5V. This measured specific on-resistance is within 20% of the analytically calculated and simulated specific on-resistance for the same device. High temperature measurements show that the threshold voltage decreases with temperature and the accumulation channel mobility (~125 $cm^2/V.s$) is almost independent of temperature. The specific on-resistance exhibited positive temperature coefficient, as opposed to the undesirable negative temperature coefficient observed on previously reported high voltage SiC MOSFETs.

I. Introduction

Silicon carbide power MOSFETs have a strong advantage over those made in silicon because the drift region can be thinner and have higher doping (for the same voltage rating) due to the higher breakdown electric field of SiC [1]. This translates into a 100 times lower specific on-resistance for SiC MOSFETs as compared to their Si counterparts. It has been shown that the MOS interface formed along the trench side walls is inferior to that formed on the Si-face of 6H-SiC [2] resulting in lower inversion layer mobilities along the trench side walls. This results in a high specific on-resistance for SiC UMOSFETs [3]. Another problem with the SiC UMOSFET is the gate oxide rupture caused by the higher electric fields in the SiC drift region. This problem is aggravated at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages [4], thus restricting the maximum operating voltage to less than half of the ideal breakdown voltage. All these obstacles have resulted in the fabricated SiC MOSFETs having specific on-resistances much higher than the ideal drift region values. Recently, high voltage 4H-SiC UMOSFETs were reported [5] which can block up to 1100V. However, due to low inversion channel mobility (1.5 $cm^2/V.s$), these devices had very high specific on-resistance of 433 $m\Omega$-cm^2 at 300K which is 125 times higher than the ideal calculated epitaxial layer specific on-resistance. DIMOS transistors on 6H-SiC with a BV of 760V and a specific on-resistance of 125 $m\Omega$-cm^2, which is 11X higher than the ideal value of the drift region, have also been reported [6]. The problems of high electric field in the gate oxide and the low channel (inversion layer) mobility have not been fully addressed with this structure. It is well known that, the accumulation layer mobility is much higher than the inversion layer mobility in silicon. Hence, assuming that the same applies to SiC, the low inversion channel mobility problem can be avoided if we use an accumulation channel, preferably on the Si-face. In a previous paper, we have proposed and experimentally demonstrated a planar vertical SiC ACCUFET structure

which eliminates both the problems of premature oxide breakdown and low inversion channel mobility [7]. In this paper, the design and optimization of the 6H-SiC ACCUFET is discussed based upon analytical models, simulations and experimental results.

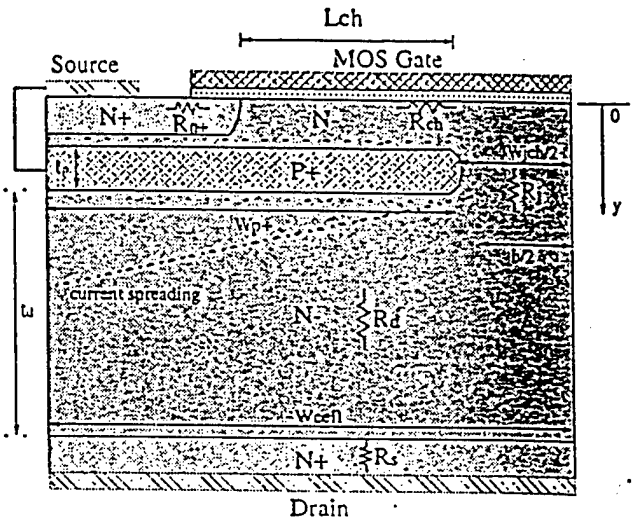

Fig.1 Schematic cross-section of the planar accumulation channel SiC vertical MOSFET. The buried P^+ is shorted to the source in the third dimension.

II. Device Structure and Operation

The basic structure of the planar ACCUFET is shown in Fig.1. In this structure, a thin N-type region is formed below the MOS gate by using a buried P^+ implanted layer resulting in an accumulation channel FET. If the threshold voltage of the ACCUFET, (V_{ta}) is defined as the gate voltage at which the bands are flat at the SiO_2/SiC interface, it can be expressed as:

$$V_{ta} = V_{bi} - V_p - V_n + \phi_{ms} - Q_{ox}/C_{ox} \qquad (1)$$

where V_{bi} is the built in voltage of the P^+-N^- junction, V_p and V_n are the voltage drops in the P^+ and N^- regions due to the band bending caused by the built in potential, ϕ_{ms} is the difference in the metal and semiconductor work functions, C_{ox} is the oxide capacitance, and Q_{ox} is the fixed

oxide charge. A positive threshold voltage ensures that the device will be normally-off and this can be achieved by varying the doping concentration and thickness of the N^- layer above the buried P^+ layer. For a given doping concentration, the maximum thickness, ($t_{n,max}$) of this N^- layer (to get a normally off device) can be derived by setting the condition that the threshold voltage is $\geq$ 0V. Using this criterion, we get the following expression for $t_{n,max}$:

$$t_{n\,max}^2 = \left(Vbi + \phi_{ms} - \frac{Q_{ox}}{C_{ox}}\right) \frac{2\varepsilon}{qN_D\left(1+\frac{N_D}{N_A}\right)} \qquad (2)$$

where N_D and N_A are the donor and acceptor concentrations in the N^- and P^+ regions. Thus, the thickness and doping of this N^- layer have to be carefully chosen such that it is completely depleted by the built-in potentials of the P^+/ N junction and the MOS gate at zero gate bias, resulting in a normally-off device.

In the ACCUFET structure, when the gate bias is zero, there is no path (channel) for the conduction of electrons from the source to the drain and the entire drain voltage is supported by the reverse biased P^+/N-drift junction. Since this P^+/N^- junction can support high voltages [8], the device is expected to have a high breakdown voltage. In the blocking mode of operation, the channel potential barrier created by the built-in potentials of the P^+/N^- junction and the MOS gate prevent any current conduction. In order to prevent the drain potential from encroaching into the channel region and lowering the channel potential barrier, the channel has to be well shielded. This can be achieved by reducing the gap between the two P^+ layers (W_{Jch}) which results in the merging of the depletion regions from the two P^+ layers at a low drain voltage and shielding the channel region from high drain voltages. Decreasing W_{Jch} also helps in reducing the electric field in the gate oxide and the field crowding at the P^+ layer edge thereby increasing the breakdown voltage (BV) of the device.

When a positive gate bias is applied, an accumulation channel (of electrons) is created at the SiO_2/SiC interface. This results in a low resistance path for the electron current flow from the source to the drain. Assuming that the higher accumulation layer mobility (as compared to the inversion layer mobility) observed in silicon applies to silicon carbide also, a lower on-resistance is expected for the planar ACCUFET. As discussed earlier, decreasing W_{Jch} is expected to reduce the maximum gate oxide electric field and increase the BV. However, when W_{Jch} is decreased, the cross-sectional area for current flow from the channel into the drift region decreases and this will result in an increase in the specific on-resistance of the device as will be explained in the following section.

Modeling of On-Resistance

The on-resistance of the planar ACCUFET is the total resistance between the source and drain terminals in the on-state. The on-resistance is an important device parameter because it determines the maximum current rating and the on-state voltage drop. The total on-resistance of the SiC ACCUFET is given by:

$$R_{on} = R_{on,sc} + R_{on,n^+} + R_{on,ch} + R_{on,j} + R_{on,d} + R_{on,s} + R_{on,dc} \qquad (3)$$

where $R_{on,sc}$ is the source contact resistance, R_{on,n^+} is the contribution from the N^+ source region, $R_{on,ch}$ is the accumulation channel resistance, $R_{on,j}$ is the contribution from the drift region between the two P^+ layers, $R_{on,d}$ is the drift region resistance, $R_{on,s}$ is the substrate resistance, and $R_{on,dc}$ is the contribution from the drain contact. In a typical high voltage device, the contribution from R_{on,n^+} is generally negligible due to the high doping and can be ignored.

The accumulation channel resistance is dependent on the charge in the accumulation layer and the mobility of the free carriers at the accumulated surface. The accumulation channel resistance is given by

$$R_{on,ch} = \frac{L_{ch}}{Z\mu_{na}C_{ox}(V_G - V_{ta})} \quad (4)$$

where L_{ch} is the channel length, μ_{na} is the accumulation channel mobility, Z is the channel width, V_G is the gate voltage and V_{ta} is the threshold voltage of the ACCUFET.

Under the assumption that the voltage drop along the vertical direction in the gap between the two P^+ layers is small enough not to change the depletion layer width, the resistance of the JFET region ($R_{on,j}$) can be calculated by finding the undepleted width (*b*) through which the current flows.

$$R_{on,J} = \frac{t_p}{q\mu_n N_D Z b} \quad (5);$$

$$b = W_{Jch} - 2\sqrt{\frac{2\varepsilon}{qN_D}V_{bi}} \quad (6)$$

where t_p is the thickness of the buried P^+ layer, N_D is the epilayer doping concentration, and μ_n is the electron mobility in the vertical direction.

To analyze the spreading resistance of the drift region ($R_{on,d}$), the drift region is assumed to begin below the bottom of the P^+ layer. The current spreads from the JFET region into the drift region. The mobility anisotropy [9] in 6H-SiC leads to excellent current spreading because the mobility in the lateral direction is 4.8X higher than that in the vertical direction. We have found that a reasonably accurate estimation of the drift region spreading resistance can be obtained by assuming that the current spreads from a cross-section of width *b* at an angle given by $\tan^{-1}(4.8)$ (=78.2°). The current flow paths overlap at a depth of $W_p/4.8$ below the P^+ layer and the drift region resistance can be modeled as the sum of a region where the cross-section for current flow increases with depth and a second region with uniform cross-section equal to the cell-width, W_{cell}. This leads to a drift region spreading resistance given by:

$$R_{on,d} = \frac{1}{9.6q\mu_n N_D Z} \ln\left[\frac{b+2W_P}{b}\right] + \frac{\left(t_d - \frac{W_P}{4.8}\right)}{q\mu_n N_D Z W_{cell}} \quad (7)$$

where t_d is the thickness of the drift region below the P^+ layer and W_P is the width of the buried P^+ layer as defined in Fig.1.

The contribution from the N^+ substrate is given by:

$$R_{on,s} = \rho_s t_s \quad (8)$$

where ρ_s is the substrate resistivity and t_s is the substrate thickness. For commercial 6H-SiC substrates, the lowest substrate resistivity currently available is about 0.1Ω-cm. The specific substrate resistance for a typical substrate thickness of 300μm, will be 3mΩ-cm² which forms a significant part of the total device specific resistance of a typical 1000V device. Hence this resistance needs to be reduced by thinning of the substrates or decreasing the substrate resistivity from what is available today.

Typically, the channel resistance and the drift region resistance are the main components that determine the total on-resistance of the device. Normally the specific on-resistance, which is the resistance of a device with unit area is used for comparison of devices. The on-resistance (R_{on}) can be converted to specific on-resistance ($R_{on,sp}$) by multiplying it by the area of the device cell ($W_{cell}.Z$) . For a typical ACCUFET device containing a 10μm thick N^- epilayer doped at 10^{16} cm^{-3} with a cell pitch of 23 μm, W_{Jch} of 4 μm and a μ_{na} of 125 $cm^2/V.s$, the calculated (using Eq.3) $R_{on,sp}$ is 18.5 mΩ-cm² which is about 2.5X that of the ideal (drift region) $R_{on,sp}$ of 7.7 mΩ-cm². This clearly shows that the proposed device has very low specific on-resistance if the accumulation channel mobility (μ_{na}) is high. In the experimental section, it will be shown that such high μ_{na} is achievable in fabricated devices.

III. Device Simulation

Two dimensional numerical simulations were done using *MEDICI* [10] for the ACCUFET structure with a 10μm thick N^- drift region doped at 10^{16} cm^{-3}. The buried P^+ layer had a Gaussian profile located between 0.3μm and 0.7μm with a peak concentration of $5x10^{13}$ cm^{-3}. An N^+ polysilicon gate electrode with a 100A thick gate oxide (Q_F =10^{11} cm^{-2}) was used. The baseline device had a cell pitch of 23μm and a channel length of about 2.5μm. The spacing between the P^+ layers, (W_{Jch}) was varied from 2 to 4μm. The simulations predicted a blocking voltage of 1550V and a specific on-resistance of 15-23 mΩ-cm^2 for the different values of W_{Jch} as described in Table.1

W_{Jch} (μm)	Simul. V_F (Volts) (L_{ch}=2.5μm)	Simul. BV (Volts) (L_{ch}=2.5μm)	Simul. $R_{on,sp}$ (mΩ-cm^2) (L_{ch}=2.5μm)	Simul. $R_{on,sp}$ (mΩ-cm^2) (L_{ch}≅7μm)	Analy. $R_{on,sp}$ (mΩ-cm^2) (L_{ch}≅7μm)	Meas. $R_{on,sp}$ (mΩ-cm^2) (L_{ch}≅7μm)	Simul. Max. E_{ox} (MV/cm)
2	2.80	1560	26.0	33.5	32.5	35.6±1.5	3.3
3	2.05	1550	20.2	26.4	26.7	28.8±1.2	4.3
4	1.85	1540	18.1	22.5	23.9	26.7±1.1	4.8

Table.1 Effect of varying the gap in the P^+ buried layer (W_{jch}) on the various device parameters. The on-state voltage drop (V_F) and specific on-resistance ($R_{on,sp}$) were obtained at a gate bias of 4V. The electric field in the gate oxide (E_{ox}) is given at a drain bias of 1500V. μ_{na}=120 cm^2/V.s was used in simulations and analytical calculations.

From the simulations, it was found that the electric field near the SiO_2/SiC interface can be controlled by adjusting W_{Jch}. When W_{Jch} is reduced, the depletion layers from the two neighboring P-N junctions merge and the region above it gets shielded from the high drain voltage, reducing the electric field under the oxide. The three-dimensional electric field profile shown in Fig.2 clearly demonstrates that while the peak electric field occurs at the edge of the P^+ layer, the electric field at the oxide interface is much less. The electric field in the drift region

below the gate oxide (in the region between the two P^+ layers) for different W_{Jch} is shown in Fig.3. It can be clearly seen that as W_{Jch} is decreased, the field at the interface decreases. It is worth pointing out that the peak electric field occurs inside the drift region at about y=1.6μm and the electric field is much lower near the SiO_2/SiC interface. Simulations predict that with $W_{Jch} \leq$ 4μm, the peak electric field in the gate oxide can be kept below 5 MV/cm (<2 MV/cm in SiC at the interface) even when the maximum electric field in SiC approaches 3 MV/cm. Thus the oxide rupture problem [3] is solved while still enabling utilization of the high breakdown electric field strength of SiC.

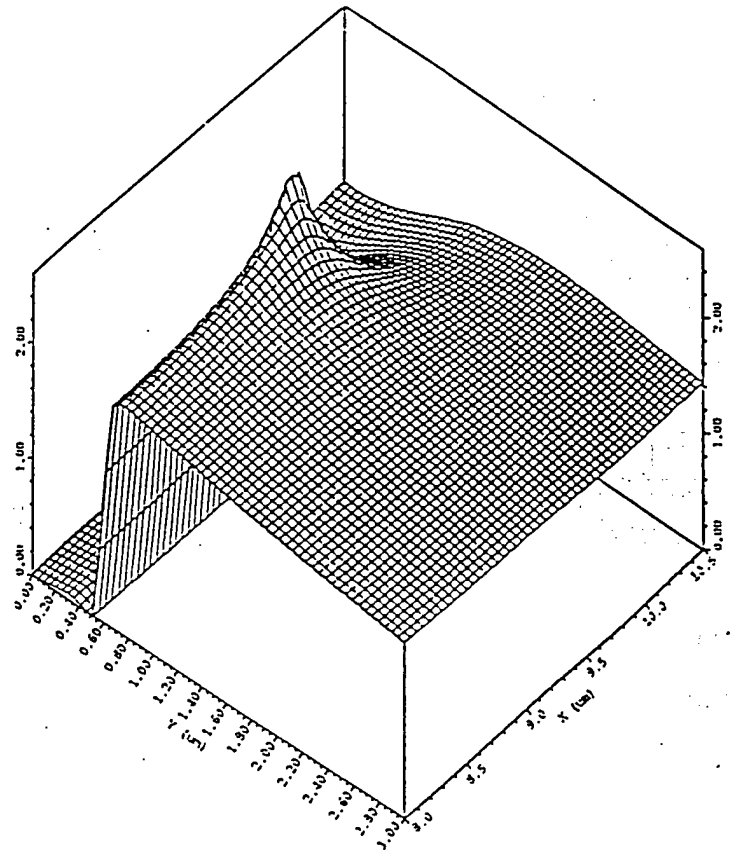

Fig.2 Simulated three-dimensional electric field profile showing the location of the peak electric field and the electric field reduction at the SiO_2 /SiC interface.

From the above discussion, it is clear that as W_{Jch} is decreased the maximum electric field in the gate oxide decreases as shown in Table.1. In contrast, it was found that varying W_{Jch} had very little effect on the breakdown voltage, changing it from 1540V to 1560V when W_{Jch} was

decreased from 4 to 2μm.This is because even for a W_{Jch} of 4μm, the depletion layer curvature is very small for an epitaxial layer doping concentration of $1x10^{16}$ cm^{-3} resulting in minimal electric field crowding at the junction edge. So reducing W_{Jch} any further will result in only negligible increase in the BV. However, when W_{Jch} is decreased, the forward voltage drop, V_F (at $100A/cm^2$) increases because the current has to now flow through a constricted region. This can be clearly seen in Fig.4 which shows current flow lines in the on-state for two cases of W_{Jch}. It may also be noted from this figure that the current spreads rapidly (~80°) once it enters the drift region due to the mobility anisotropy effect which was discussed earlier. The effect of changing W_{Jch} on the V_F is given in Table.1. Thus, there is a trade off between reducing the forward voltage drop by increasing W_{Jch}, and reducing the maximum gate oxide field by decreasing W_{Jch}. Based on the simulation results, an optimum value for W_{Jch} of 3μm gives a good compromise between obtaining low V_F and E_{ox}.

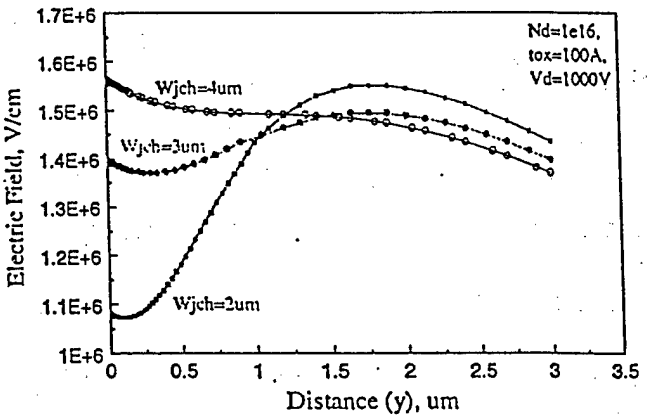

Fig.3 Effect of the size of the gap in the P^+ buried layer (W_{Jch}) on the electric field profile below the gate oxide in the region between the gap in the P^+ buried layer. These profiles were obtained at a drain bias of 1000V. The SiO_2 /SiC interface is located at y=0.

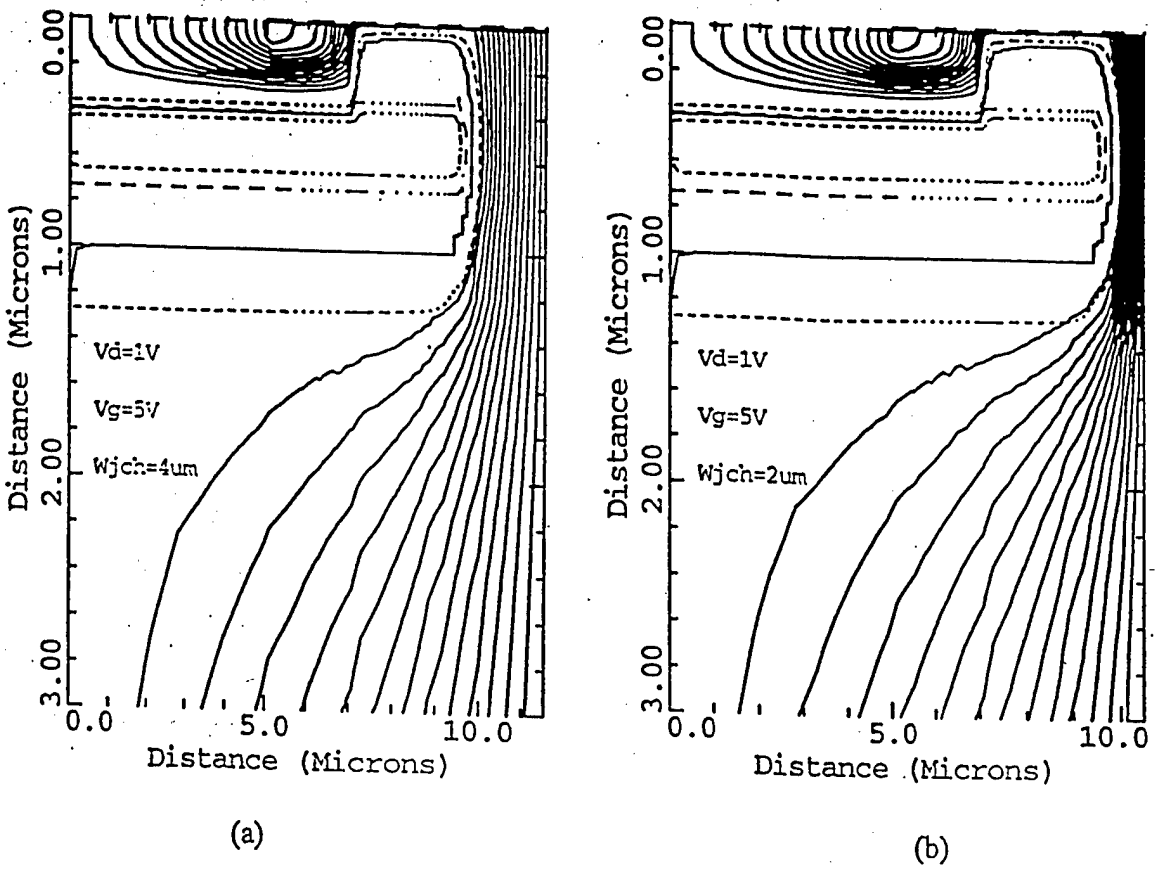

Fig.4 Simulated current flow lines under on-state condition (Vg=5V, Vd=1V) for (a) W_{Jch}=4μm, (b) W_{Jch}=2μm.

IV. Device Design and Fabrication

After verifying the concept of the planar SiC ACCUFET through two-dimensional simulations, devices were designed to experimentally demonstrate their operation. The devices were designed with various geometrical cell design parameters with an inter-digitated linear geometry using 2μm design rules. The baseline device had a cell pitch of 23μm with a W_P^+ of 19μm. While some designs had metal finger contacts on the N^+ source, other designs just had a metal contact on the N^+ source pad area. Hence for those devices with remote source contact, the N^+ sheet resistance also gets added on to the total device resistance. No termination structure is used for all the devices.

Single crystal N-type ($2x10^{18}$ cm^{-3}) 6H-SiC substrates [11] with 10μm thick nitrogen doped (10^{16} cm^{-3}) epitaxial layers were used to fabricate the planar ACCUFETs. The buried junction was formed by a single high energy (380 KeV) boron implantation at a dose of $1x10^{14}$ cm^{-2}. Monte Carlo simulations using SUPREM III predicted a channel thickness of about 0.3μm and a junction depth of 0.7μm which was confirmed by SIMS measurements. This implant was followed by multiple lower energy boron implants (30,100,200KeV) at the pad area so that contact could be made to the buried layer and at also the periphery to isolate the source from the drift region at the edges of the device. Multiple energy (40,100KeV) nitrogen implants at a dose of $8x10^{14}$ cm^{-2} was used to form the N^+ source regions. All implants were annealed at 1400 °C in argon for 30 minutes. After a standard RCA clean, the gate oxide was thermally grown using wet oxidation at 1100 °C followed by re-oxidation at 950 °C to reduce D_{it} and Q_f [12]. A 0.5μm thick polysilicon was deposited by LPCVD and doped with phosphorus at 875 °C. The polysilicon was patterned using SF_6/O_2 RIE and isolation oxide was thermally grown on the patterned polysilicon. Ti/Al was used to form both front and back side ohmic contacts [13].

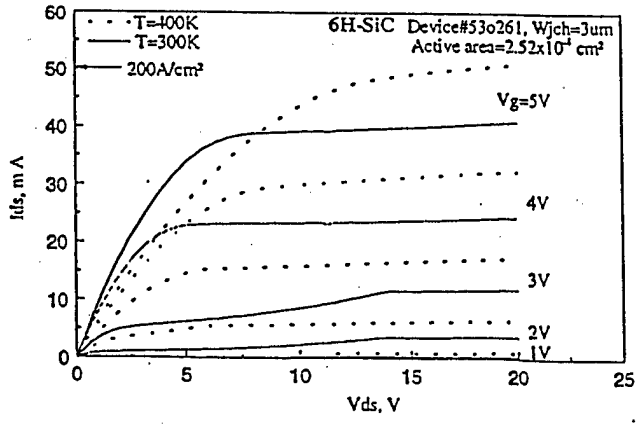

Fig.5 This figure shows the effect of temperature on the measured output characteristics of a typical 6H-SiC ACCUFET

V. Experimental Results and Discussion

Capacitance -voltage measurements on MOS capacitor test elements gave a gate oxide thickness of 125 A and a fixed oxide charge of ~10^{12} cm^{-2}. The N^+ source sheet resistance was measured to be 2.2KΩ/sq. at room temperature which is in reasonable agreement with the expected (simulation) value of 1.5KΩ/sq; the slightly higher value is probably due to the incomplete activation of dopants at this annealing temperature.

The buried P^+ layer was shorted to the source during all the measurements. Excellent I-V characteristics were obtained on the fabricated planar ACCUFETs with good current saturation and gate control as shown in Fig.5. The unterminated devices had a breakdown voltage (BV) of 350V with a leakage current of <100 μA just before breakdown. There was no deterioration in the BV with repeated measurement on the same device as long as the current at breakdown was limited to 5 mA (20A/cm^2). The gate current was monitored during BV measurement and found to be <1nA even during the device breakdown. This demonstrates that the breakdown is non-catastrophic and the gate oxide rupture, which has been a major problem in SiC UMOSFETs [4], is prevented. A room temperature specific on-resistance ($R_{on,sp}$) of 18 mΩ-cm^2 was measured on the best device (cell pitch = 21μm, W_{Jch} = 4μm and L_{ch} = 2.5μm) at a gate bias of only 5V. Thus, the fabricated ACCUFETs have excellent on-state conduction even with the low (logic-level) gate voltages. In contrast, most of the previous SiC MOSFETs [4,5,14] have used high voltage (25-60V) gate drive in order to obtain on-state conduction which is usually unacceptable in power electronic systems. It may also be pointed out that the ACCUFET device can carry extremely high currents (>300A/cm^2) even when operating at a small gate bias of 5V. Hence these ACCUFETs can be operated at high current densities resulting in smaller device areas, higher yield and lower cost.

The specific on-resistance of this device is much lower than that of the previously reported best 6H-SiC 50V UMOSFET (38 mΩ-cm²) [15] and the best 6H-SiC DIMOSFET (760V, 125 mΩ-cm²) [6]. The calculated specific on-resistance for the drift region in the fabricated ACCUFET devices is 7.7 mΩ-cm². Thus, the measured specific on-resistance for the planar ACCUFET device is within 2.5X of the drift region which can support over 1500V. We believe that this is the best value obtained so far for any high voltage SiC MOSFET structure.

As mentioned earlier, while some designs had metal finger contacts on the N^+ source, other designs just had a metal contact only on the N^- source pad area to reduce the likelihood of gate to source shorts. It was observed that the devices with source metal fingers had low $R_{on,sp}$, typically < 25 mΩ-cm² whereas those with remote source contacts had higher $R_{on,sp}$, in the range of 200 mΩ-cm². This was expected because for those devices with remote source contact, the N^+ sheet resistance (which is high) gets added on to the total device resistance. The effect of this high sheet resistance can be accounted for by modeling the current flow through the N^+ source finger in the z-direction. The voltage along the N^+ source finger will increase as z increases. An expression for this voltage V(z) can be derived under the following assumptions: (i) The N^- source finger sheet resistance is uniform, (ii) $V_{DS} << V_{GS}$ (true in the on-state) and therefore the MOS channel resistance remains constant, (iii) the drift region resistance is constant.

$$V(z) = V_{DS}(1 - e^{-kz}) \tag{9}$$

$$\text{where} \quad k = \sqrt{\frac{R_{sh}}{W_{N^+} R_{dev}}} \tag{10}$$

where R_{sh} is the N^+ source finger sheet resistance, W_N^+ is the width of the N^- source finger, and R_{dev} is the device resistance per unit length for R_{sh}=0. This expression is derived under the

assumption that $k.L_N^+$ is large ($e^{-kL_n^+} \cong 0$), where L_N^+ is the length of the N^+ source finger. Using this equation, the ratio of the total specific on-resistance with and without R_{sh} is given by

$$\frac{R_{on,sp}(R_{sh} \neq 0)}{R_{on,sp}(R_{sh} = 0)} = kL_N^+ \qquad (11)$$

For a typical device with R_{sh}=2.2KΩ/sq., W_N^+ =6.5μm, and L_N^+ =150 μm, we get $k.L_N^+$ = 9.5. This means that the devices with out source metal fingers will have 9.5 times higher $R_{on,sp}$ than identical devices with source metal fingers. This is consistent with the values of ~20 mΩ-cm² and ~200 mΩ-cm² measured for the devices with and without metal fingers.

Measurements were done on devices with different W_{Jch} and specific on-resistances ($R_{on,sp}$) was determined. Since these devices had only remote source contact, the correction factor ($k.L_N^+$) was used in extracting the $R_{on,sp}$. It was observed that as W_{Jch} was increased, $R_{on,sp}$ decreased as expected. The measured specific on-resistances for the different W_{Jch} along with the simulated and analytically calculated values are given in Table.1. In the simulations and analytical calculations, the contribution from the substrate resistance was neglected. This was done because in the measured devices, the effective substrate resistance is very small (<5% of the usual $R_{on,s}$) due to wafer level probing which leads to current spreading in the substrate. It may be noted although the measured value is slightly higher, possibly due to contributions from the contact resistances, there is good agreement between these values.

The threshold voltage V_{th} and the accumulation channel mobility μ_{ns} was extracted from the transfer characteristics shown in Fig.6. The intercept on the X-axis of this plot gives the threshold voltage which was extracted to be +0.76V at room temperature (300K). From the slope of this plot, the effective room temperature accumulation channel mobility was calculated to be 120 cm²/V-s. It is worth pointing out that this value is higher than the highest reported inversion layer mobility (72 cm²/V-s) in lateral 6H-SiC MOSFETs [12] and much higher than values

obtained in vertical power device structures [4-6] leading to low specific on-resistance for the ACCUFET.

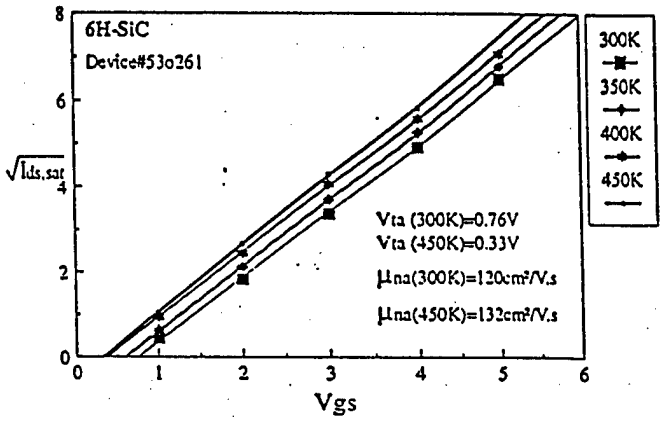

Fig.6 Measured transfer characteristics of a typical device for different temperatures.

High Temperature Characteristics

The devices were characterized at elevated temperatures (up to 450K) to observe the effect of temperature on the device performance. It can be seen from the high temperature output characteristics shown in Fig.5 that both the on-resistance and the saturation current increases with temperature.

The dependence of the threshold voltage on temperature was also measured. As expected, the V_T decreases from 0.76 V at room temperature to 0.33V at 450K (~ -3 mV/°C) as can be seen from the Fig.6. The effective accumulation channel mobility extracted from the plot increased slightly from 120 to 132 cm^2/V-s when the temperature was increased from 300K to 450K. However, on a similar device, the accumulation channel mobility decreased slightly from 125 to

120 cm^2/V-s for the same temperature range. These changes are too small and fall within the measurement and extraction error and hence no definitive trend in the effective accumulation channel mobility with temperature could be obtained. So it may be concluded that the accumulation channel mobility in these devices remains almost independent of temperature, unlike inversion layer mobility which increases rapidly with temperature [16] giving rise to the undesirable negative temperature coefficient of on-resistance for the inversion channel power devices reported in the literature [5].

The variation of the specific on-resistance as a function of temperature (300-450K) was measured. It was seen that while some devices showed an increase in $R_{on,sp}$ with temperature, some showed a slight decrease with temperature as shown in Fig.7. Analysis of the design variations of these devices showed that all the devices which had source metal fingers (and hence low $R_{on,sp}$) exhibited a positive temperature coefficient whereas those which had remote source contacts showed a negative temperature coefficient. The $R_{on,sp}$ of the devices with source metal fingers had a temperature dependence of T^n where n varied from 1.4 to 1.73 for the different devices. Measurements on test elements show that the drift region also has a positive temperature coefficient as shown in Fig.7 with an n value of 1.82 which is consistent with published values [17]. Although the electron mobility in 6H-SiC varies as T^{-n} where n=2.5 [18], the $R_{on,sp}$ does not increase with an n value of 2.5 because of the increase in the carrier concentration due to the improved dopant ionization at higher temperatures. If the total on-resistance of the device was composed of only the drift region resistance, the device also would have an n of 1.82. However, the total device resistance consists of other components such as the channel, contact, substrate resistance etc. (Eq.3) and the fact that the device resistance had an $n < 1.82$ shows that these components collectively have a lower ($n<1.82$) temperature dependence. The most important point to be noted is that these devices have a strong positive temperature coefficient unlike

previous SiC MOSFETs [5]. A positive temperature coefficient is extremely desirable since it allows paralleling of devices and also improves reliability by avoiding current filamentation problems.

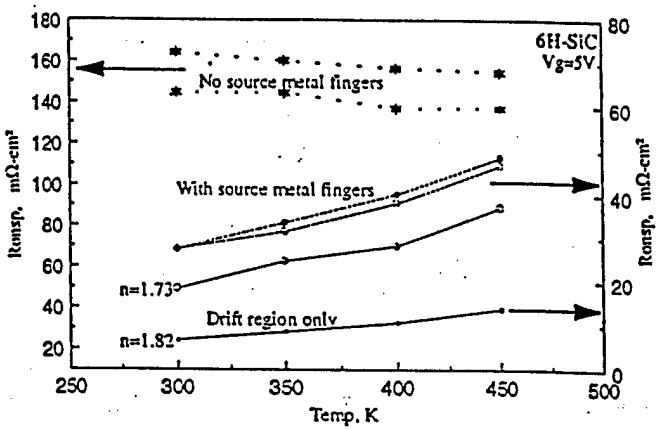

Fig.7 Specific on-resistance for the two sets of devices and that of the drift region measured as a function of temperature.

As mentioned earlier, the devices with remote source contact had a slight negative temperature coefficient. It is possible to get a negative temperature coefficient only if one of the components have a negative temperature coefficient. The N^+ source sheet resistance was measured as a function of temperature and it was revealed to have a negative temperature coefficient with an n value of -1.25 resulting in a negative temperature coefficient for the total specific on-resistance for these devices.

VI. Conclusions

In this paper, the characteristics of the planar 6H-SiC ACCUFET have been analyzed. Two-dimensional numerical simulations show that this structure does not suffer from the gate oxide

rupture problem prevalent in SiC UMOSFETs and also has a low specific on-resistance (2X of ideal). Simulations show that the maximum electric field in the gate oxide can be reduced by decreasing the gap between the P^+ buried layers (W_{Jch}), but at the expense of an increase in the specific on-resistance. The fabricated devices had extremely good current saturation and low measured specific on-resistance of 18 $m\Omega$-cm^2 at a gate bias of only 5V. A high accumulation channel mobility of about 120 $cm^2/V.s$ was experimentally measured on the fabricated devices. Due to the high channel conductance and low specific on-resistances, these ACCUFETs can be operated at high current densities resulting in smaller device areas, higher yield and lower cost. The simulations predicted a decrease in the specific on-resistance with increasing gap between the P^+ buried layers (W_{Jch}) which was confirmed by experimental results. The specific on-resistance was demonstrated to have a positive temperature coefficient which is highly desirable for power devices.

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VII. Comparison of 6H-SiC and 4H-SiC High Voltage Planar ACCUFETs

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Abstract

SiC switches are extremely promising for high power applications, such as UPS and motor control, because of extremely low power losses as compared to Si devices. Although very low diffusion coefficients in SiC has motivated the fabrication of UMOSFETs, the performance of these devices has been limited by premature oxide breakdown and low inversion layer mobility. A novel planar vertical MOSFET structure (called ACCUFET), which eliminates both these problems, has been demonstrated by us. In this paper, we compare characteristics of ACCUFETs fabricated from 6H-SiC and 4H-SiC polytypes. A room temperature specific on-resistance ($R_{on,sp}$) of 18 mΩ-cm^2 was measured on the best 6H-SiC device (designed for a breakdown voltage of 1500V) at a logic-level gate drive voltage of only 5V, which was in excellent agreement with 15 mΩ-cm^2 obtained in simulations. The $R_{on,sp}$ exhibited a positive temperature coefficient. In contrast, the room temperature $R_{on,sp}$ for the best 4H-SiC reduced rapidly with increase in temperature to 128 mΩ-cm^2 at 450 K. At room temperature, the unterminated 6H-SiC and 4H-SiC devices had a breakdown voltage (BV) of 350V and 450 V, respectively, with a leakage current of < 100 μA. However, a breakdown voltage of 1240V is obtainable from the epitaxial material on using an Ar implant (amorphization) edge termination.

Introduction

The specific on-resistance of SiC FETs has been projected to be 100X lower than Si devices. Due to very low diffusion coefficients in SiC even at high temperatures, the UMOS structure has been used to fabricate 4H-SiC MOSFETs with breakdown of 1.1 kV [1]. In a SiC UMOS structure, high electric field at the trench corners leads to catastrophic failure of the gate oxide at high drain voltages [2], which restricts the maximum operating voltage to much below the plane parallel breakdown voltage. Further, the extremely low (1-7 cm^2/V-s) inversion layer mobility observed in the SiC UMOS devices leads to a high specific on-resistance for the device, which nullifies the advantage of the low drift region resistance. A novel planar vertical MOSFET structure (called ACCUFET), which eliminates both the problems of premature oxide breakdown and low inversion layer mobility, has been demonstrated by us [3]. In this paper, we compare the characteristics of ACCUFETs fabricated from 6H-SiC and 4H-SiC polytypes with measured breakdown voltages of 350-450 Volts.

Device Structure

Fig.1 shows the cross-section of the proposed structure. The thickness and doping of the N layer below the gate oxide is chosen such that it is completely depleted by the built-in potentials of the P^+/N^- junction and the MOS gate, resulting in a normally-off device with the entire drain voltage supported by the P^+/N^- drift junction. The device is expected to have high breakdown voltage as this implanted P^+/N^- junction can support high voltages. The structure also utilizes the buried P^+ region to suppress the electric field below the gate oxide, thereby preventing oxide rupture.

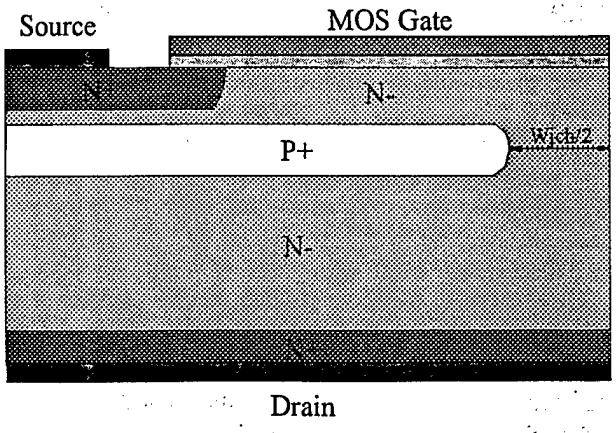

Fig. 1 Schematic cross-section of the planar SiC ACCUFET

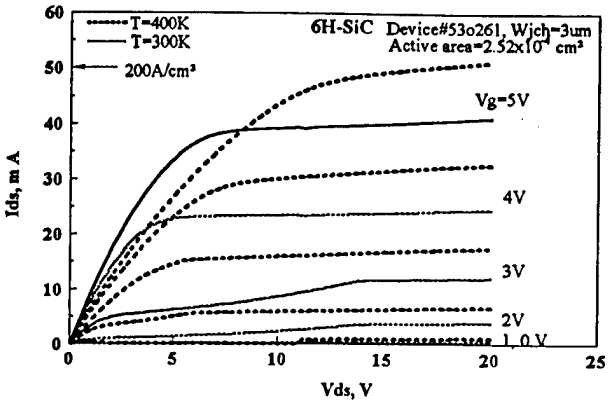

Fig. 2 Effect of temperature on the output characteristics of a 6H-SiC planar ACCUFET.

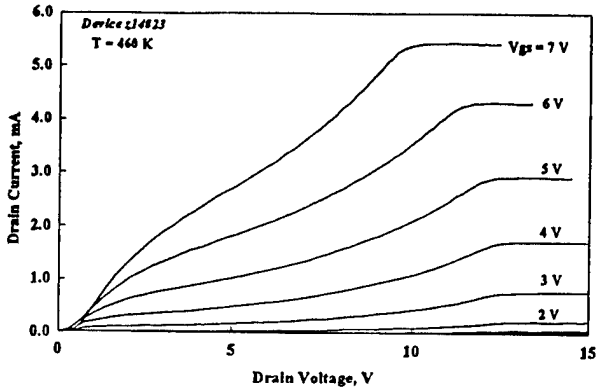

Fig. 3 Measured output characteristics of a 4H-SiC planar ACCUFET at 460 K.

When a positive gate bias is applied, the electrons flow through an accumulation channel created at the SiO_2/SiC interface. Since the accumulation layer mobility is expected to be higher than the inversion layer mobility, a lower on-resistance is expected for the proposed device. In order to verify the device operation, two dimensional numerical simulations were done using *MEDICI*. Simulations predicted that, with Wjch $\leq$ 4 μm, the peak electric field in the gate oxide can be kept below 3.5 MV/cm even at a high drain bias of 1000V, thus preventing the oxide rupture problem observed in UMOSFETs [1,2].

Device Fabrication

An 8 mask process was developed to fabricate the high voltage planar ACCUFETs. The starting wafers for both 6H- and 4H-SiC were single crystal N-type ($3x10^{18}$ cm^{-3}) substrates with a 10 μm thick nitrogen doped (10^{16} cm^{-3}) epilayer. The buried junction was formed by a single high energy (380 KeV) boron implantation at a dose of 1 x 10^{14} cm^{-2}. Monte Carlo simulations using SUPREM III predicted a channel thickness of about 0.3 μm and a junction depth of 0.7 μm. This implant was followed by multiple lower energy boron implants at the pad area so that contact could be made to the buried layer and at the periphery to isolate the source from the drift region at the edges of the device. Multiple energy (40,100 KeV) nitrogen implants at a dose of 8 x 10^{14} cm^{-2} were introduced to form the N^+ source regions. All implants were annealed at 1400 °C in argon for 30 minutes. After a standard RCA clean, the gate oxide (12.5 nm for 6H-SiC and 16 nm for 4H-SiC) was thermally grown using wet oxidation at 1100 °C followed by re-oxidation at 950 °C to reduce D_{it} and Q_f [4]. A 0.5-μm thick polysilicon was deposited by LPCVD and doped with phosphorous at 875 °C. The polysilicon was patterned using SF_6/O_2 RIE and isolation oxide was thermally grown on the patterned polysilicon. Ti/Al was used to form both front and back side ohmic contacts. The ACCUFETs were fabricated with interdigitated linear geometries using 2-μm design rules.

Results and Discussion

All the characterization was done with the buried P^+ layer shorted to the source. Excellent I-V characteristics (Fig. 2) were obtained on the fabricated planar 6H-SiC ACCUFETs with good current saturation and gate control. Both the specific on-resistance ($R_{on,sp}$) and the saturation current increased with the temperature. A room temperature $R_{on,sp}$ of 18 mΩ-cm^2 was measured on the best 6H-SiC device (cell pitch = 21 μm, W_{jch} = 4 μm and L_{ch} = 2.5 μm) at a logic level gate bias of only 5V, which was in excellent agreement with 15 mΩ-cm^2 obtained in simulations. In contrast, most of the previous SiC MOSFETs have used high-voltage (> 25V) gate drive in order to obtain good on-state conduction. In spite of using a low gate voltage, the measured specific on-resistance of our 6H-SiC ACCUFETs is lower than that of the best 6H-SiC 50V UMOSFETs (38 mΩ-cm^2) [6] and the best 6H-SiC DIMOSFET (510V, 66 mΩ-cm^2) [7]. The measured $R_{on,sp}$ for the 6H-SiC ACCUFET is within 2.5X of the measured drift region resistance which is the best value obtained so far for any high voltage SiC MOSFET. Further, this $R_{on,sp}$ is 30× lower than that of a 1500V Si MOSFET. The $R_{on,sp}$ in the 6H-SiC devices exhibited a small positive temperature coefficient, which is relevant for paralleling and reliability of devices.

The I-V characteristics of the 4H-SiC ACCUFET exhibit larger $R_{on,sp}$ (Fig. 3). The room temperature $R_{on,sp}$ for the best 4H-SiC device was found to be very high (3.2 Ω-cm^2 at a gate bias of 5V), but reduced rapidly with increase in temperature to 128 mΩ-cm^2 at 450 K

(Fig.4(a)). The reduction in $R_{on,sp}$ of the 4H-SiC devices was found to be due to an exponential increase of the effective channel mobility from 0.06 cm^2/V-s at room temperature to 2.3 cm^2/V-s at 450 K (Fig. 4(b)). The specific on-resistance is expected to be lower for devices fabricated on 4H-SiC wafers than those on 6H-SiC wafers due to the higher bulk mobility for electrons. Measurements on the test elements showed that as expected, the drift region resistance is indeed lower on the 4H-SiC wafers (0.9 $m\Omega$-cm^2 vs 7.7 $m\Omega$-cm^2 for 6H-SiC). Hence, it was concluded that the high resistance is most probably caused by the channel. The SIMS profile (Fig. 5) of the deep boron implant indicated that the desired N-layer is formed for 6H-SiC. However, the SIMS profile exhibited a "shoulder" near the SiC/SiO_2 interface for 4H-SiC. This indicates that the surface may have been inverted to P-type for 4H-SiC, which suggests formation of an inversion channel in the 4H-SiC MOSFET during the on-state. The increase in effective channel mobility with temperature for 4H-SiC is believed to be caused by interface states which trap electrons from the inversion layer. In comparison, the effective accumulation channel mobility in a 6H-SiC planar ACCUFET was extracted to be 120 cm^2/V-s indicating much less trapping.

At room temperature, the unterminated 6H-SiC and 4H-SiC devices had a breakdown voltage (BV) of 350V and 450 V, respectively, with a leakage current of < 100 μA (Fig. 6). Unlike the SiC UMOSFET, no evidence of oxide rupture was observed at breakdown in the SiC ACCUFET. Breakdown voltage of the buried P^+/N^- junction improved from 510V to 1240V on using an Ar implant edge termination [8], indicating that breakdown voltages of 1240V are obtainable from the epitaxial material used for fabricating the above ACCUFETs. Reverse breakdown characteristics of the buried P^+/N^- junction with and without the edge termination are shown in Fig. 7. Notice that the breakdown voltage improves with increase in the ion implanted area.

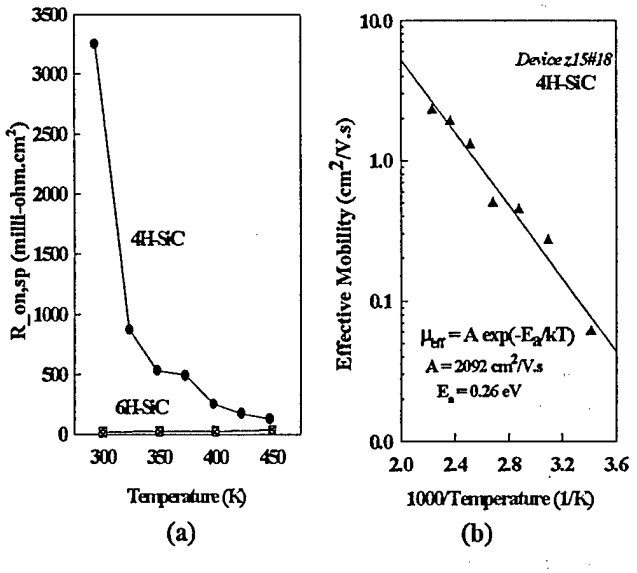

Fig. 4 (a) Effect of temperature on the specific on-state resistances in 6H- and 4H-SiC planar ACCUFETs. (b) Variation of effective mobility in a 4H-SiC planar ACCUFET with temperature, exhibiting Arrhenius-type dependence.

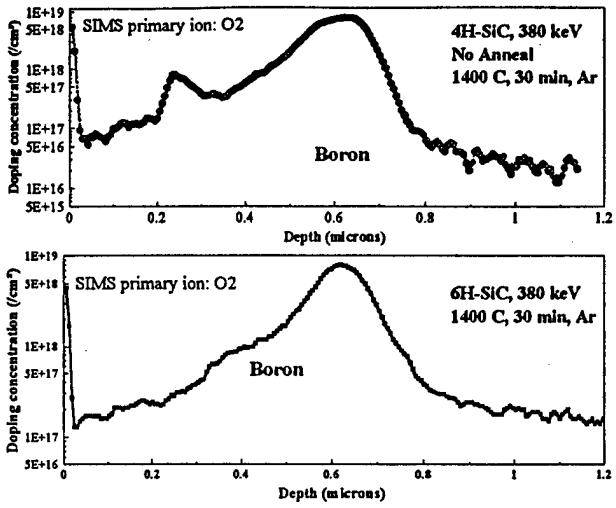

Fig. 5 SIMS profiles of deep boron ion implant in 4H-SiC and 6H-SiC.

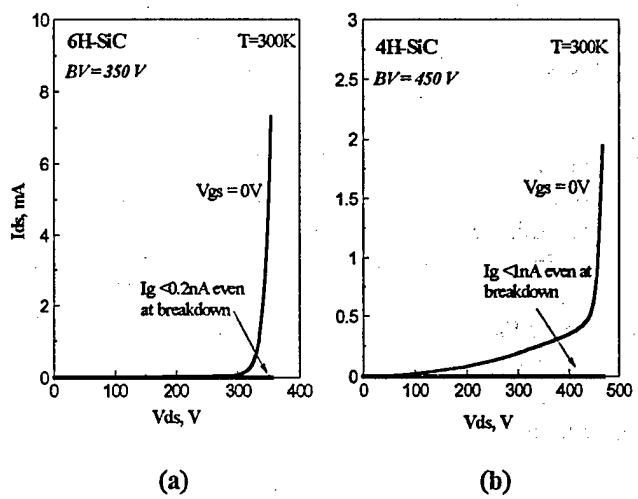

Fig. 6 Experimentally measured blocking characteristics of (a) 6H-SiC and (b) 4H-SiC planar ACCUFETs showing a BV of 350V and 450V, respectively.

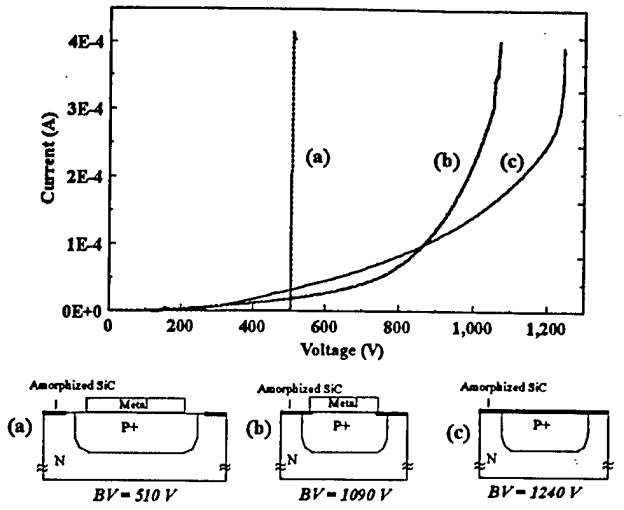

Fig. 7 Reverse I-V characteristics of the P^+/N^- diode of the ACCUFET with and without edge termination using amorphization. Breakdown voltage of upto 1240 V were measured after argon implant edge termination.

In Fig. 8, we compare specific on-resistance and breakdown voltage of 4H- and 6H-SiC ACCUFETs with other SiC MOSFETs. For reference, lines describing the variation of specific on-resistance with breakdown voltage are included for Si (at 25 °C), Si (at 175 °C) and SiC. The unterminated 4H-SiC ACCUFET (3.2 Ω-cm^2, 450V) is above the Si limit at room temperature. However, at 175 °C, this device is close to the Si limit, assuming no change in the breakdown voltage. At this temperature, after edge termination, the 4H-SiC ACCUFET is about 10X better than the best Si device. The unterminated 6H-SiC ACCUFET is at the Si limit even at room temperature. After edge termination, this device is 100X better than the best Si device.

Conclusions

Planar high voltage vertical SiC ACCUFETs were fabricated from both 6H- and 4H-SiC using a buried implanted region which shields the gate oxide, thereby preventing the oxide rupture problem prevalent in SiC UMOSFETs. The 6H-SiC transistors had extremely good current saturation and low measured specific on-resistance of 18 mΩ-cm^2 at a logic level gate bias of only 5V. The 4H-SiC device exhibited higher measured specific on-resistance, which decreased rapidly with temperature.

Acknowledgements

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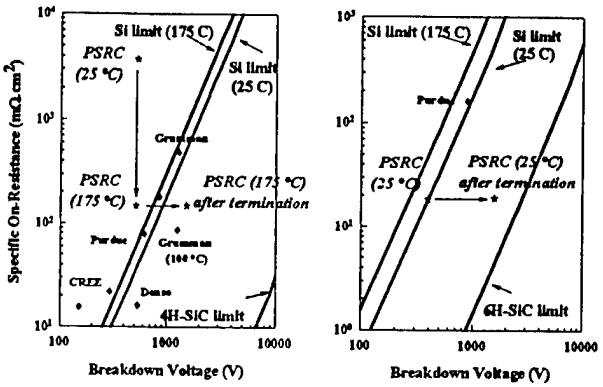

(a) 4H-SiC (b) 6H-SiC

Fig. 8 Comparison of SiC Power MOSFETs.

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Design and Development of Process Routes Leading to 4"-diameter SiC Substrates

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Introduction

The primary goal of this research is to develop fabrication techniques for the production of large-area, low-defect density, device-quality SiC films on Si substrates. Currently available commercial SiC substrates have diameters ≤ 2". It is, therefore, desirable for SiC substrates to be produced in already existing 4"-diameter Si processing equipment. To this end, three candidate processing routes were determined: (1) the conversion of the near surface region of Si(111) or SIMOX (111) surfaces to SiC for subsequent homoepitaxial growth of a thick SiC layer, (2) the use of an (0001) oriented AlN interlayer deposited on a thin converted layer of SiC for subsequent growth of SiC, and (3) the utilization of lateral epitaxial overgrowth (LEO) techniques.

During the past year, the group has accomplished the following tasks towards the completion of the goals of this project. Firstly, significant research was conducted on the conversion of Si(111) surfaces to SiC. Multiple characterization techniques were used in the chemical and microstructural analysis of the converted layers produced. X-ray photoelectron spectroscopy (XPS), scanning electron microscopy (SEM), and reflective high-energy electron diffraction (RHEED) investigations were conducted on the SiC layers at NCSU while transmission electron microscopy (TEM) and spectroscopic elipsometry studies were carried out elsewhere. Twinning was observed in the initially produced SiC layers, and the converted layer contained pits and blisters. Efforts to optimize the conversion process have resulted in converted layers free of both twinning and blisters. It is expected that pit-free layers will be produced in the next few months. Conversions were subsequently conducted on SIMOX (111) substrates. Multiple characterization techniques were employed. The initial layers of SiC produced on SIMOX were also poor in surface quality containing both pits and blisters. As in the case of the converted layers on Si(111), efforts to optimize the conversion process on SIMOX resulted in layers free of blisters.

Work has also been completed regarding the growth of AlN interlayers on Si(111) for the subsequent growth of SiC(111) layers. Films of AlN have been grown on SiC converted layers; however, the surface quality of the AlN has been poor. This is reflective of the quality of the converted layers themselves which contain pits.

Finally, a chemical vapor deposition (CVD) system is being retrofitted specifically for the growth of SiC films. The system contains a RHEED chamber to allow determination of the film polytype. The sample is RF heated to allow growth temperatures of 1500°C to be achieved. The system will be capable of handling wafers to 1.5" in diameter.

Major Results and Findings

Conversion of Si(111) and SIMOX (111) to SiC(111)

A gas source molecular beam epitaxy (GSMBE) system has been used to convert a thin surface layer of a Si(111) substrate to cubic 3C-SiC(111). The system has a base pressure better than 1E-9 Torr and a processing pressure between 1E-5 Torr and 5E-5 Torr. Ethylene (C2H4) is used as the carbon source for the conversion with flow rates between 0.2 and 2.4 sccm. The surface temperature of the sample is between 860°C and 1100°C, and conversion times range between 15 and 60 minutes.

The best converted surfaces on Si(111) substrates have been obtained with low conversion temperatures and low carbon fluxes. A RHEED pattern and SEM micrograph of a representative surface may be seen in Figure 1. This surface was produced on a Si(111) on-axis substrate with an ethylene flow rate of 0.2 sccm and a surface temperature of 860°C. A temperature ramp up rate of 30°C/min was used along with a dwell time of 30 minutes. It can be seen from the SEM micrograph that while the surface contains triangular pits, no blisters are present. Figure 2 shows an SEM micrograph of a converted Si(111) surface which contains both pits and blisters. This surface was converted using both a high-temperature (1100°C) and a high carbon flux (1.8sccm). It is clear from comparison of the two micrographs that the surface converted under the low-temperature/low-flux regimen has better surface quality. Figure 3 shows the interface between the substrate and the converted layers. It can be seen here that the rough interface exists between the substrate and the converted layer.

The best converted surfaces on SIMOX (111) substrates were also obtained utilizing low processing temperatures and low carbon fluxes. Figure 4 contains an SEM micrograph showing such a surface. While the surface does contain triangular pits similar to those seen in the converted surfaces on Si(111), it does not contain blisters. It is

thought that the pits observed in the converted layers of both Si(111) and SIMOX (111) are the result of a cleaning artifact. Through experimenting with different surface cleaning techniques, it is expected that pit-free converted layers will be achieved.

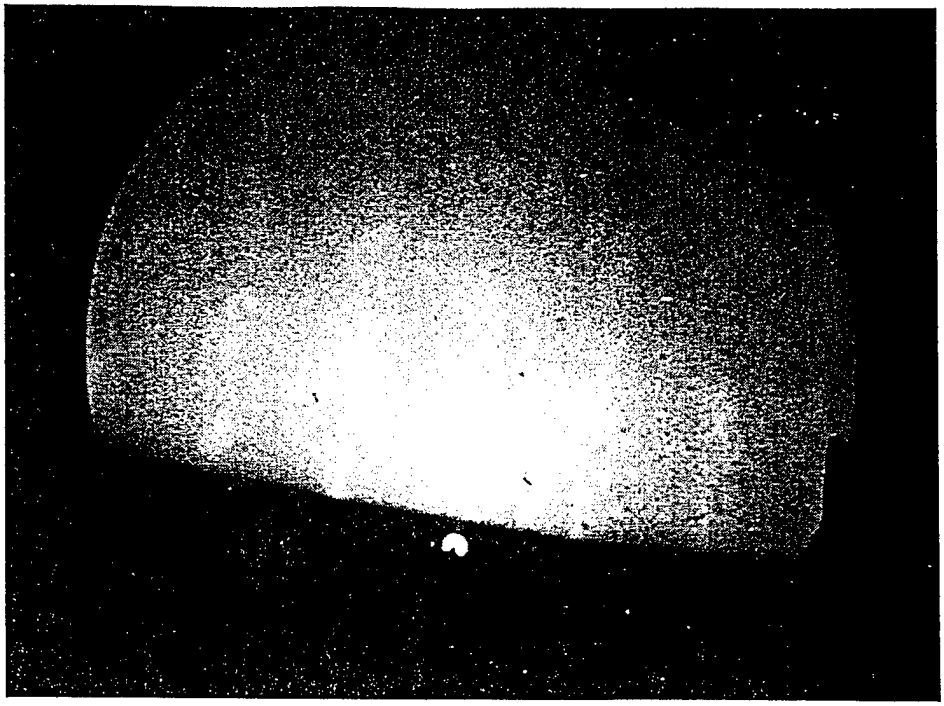
Crystalline Interlayer Deposition

A chemical vapor deposition (CVD) system is used to deposit a layer of crystalline AlN on top of which a thick layer of SiC may be grown. The system has a base pressure of 45 Torr, and growth temperatures of 1100°C. Growth times of 90 minutes or more are used. Triethylaluminum (TEA) is used as the aluminum source with a flow rate of 26 μmol/min. Ammonia is used as the nitrogen source with a flow rate of 1500 sccm. Hydrogen is used as a carrier gas and diluent with a flow rate of 3000 sccm. AlN layers have been grown on both Si(111) and on converted SiC(111) layers. Figures 5 and 6 show both RHEED patterns and SEM micrographs of AlN layers grown on both Si(111) and on SiC, respectively. It can be seen from the micrographs that the pits in the converted SiC layers show through in the AlN layers. Figure 7 shows a TEM micrograph of interfaces between the Si substrate, the SiC converted layer, and the AlN interlayer.

As part of the second and third year project goals, it is expected that using the new CVD system, which is currently under construction, SiC will be grown on the AlN interlayers.

Lateral Epitaxial Overgrowth (LEO) Techniques

A new chemical vapor deposition (CVD) system is being retrofitted specifically for work on this project. The new system will enable the conversion of both Si(111) and SIMOX (111) surfaces to SiC, homoepitaxial growth of SiC, growth of AlN interlayers, and growth of SiC on top of the AlN interlayers. In addition, it will allow for experimentation with lateral epitaxial overgrowth techniques. It is expected that this system will come on line the beginning of next year (1999). A schematic of the system can be seen in Figure 8.



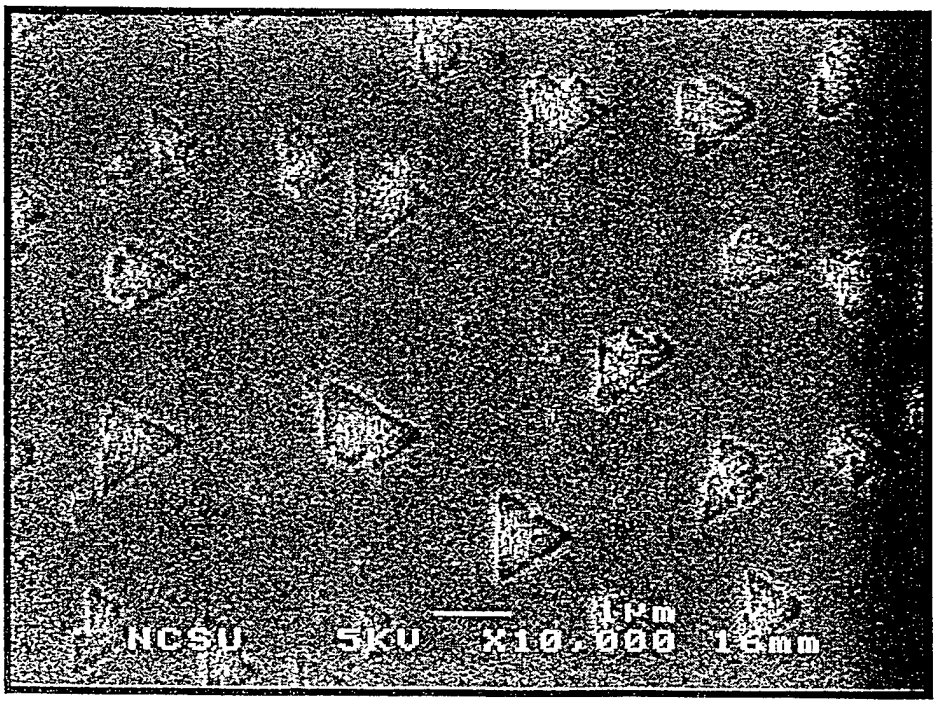


Figure 1. Low temperature/low flux SiC conversion on Si(111) RHEED and SEM.

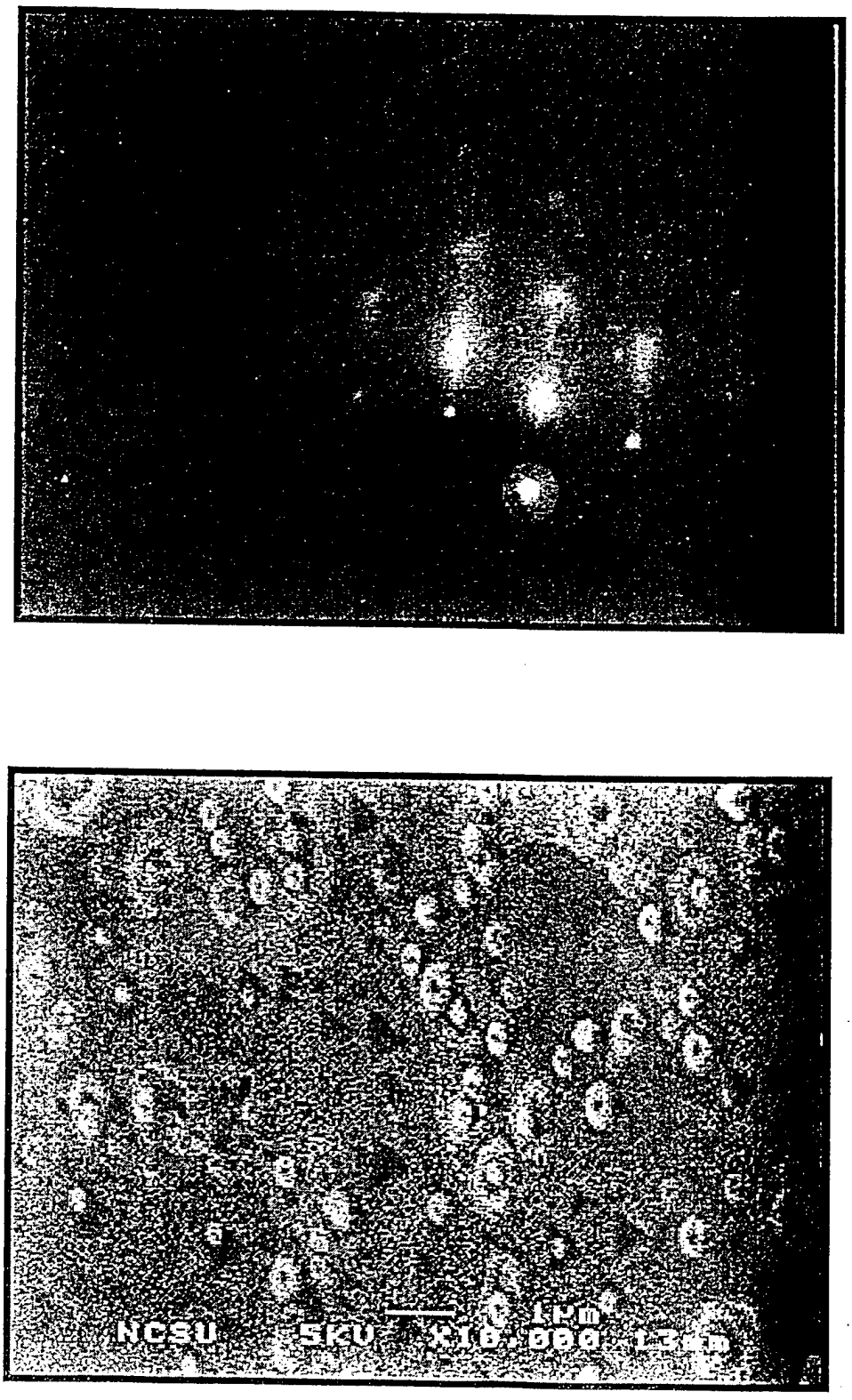


Figure 2. SEM of conversion with pits and blisters.

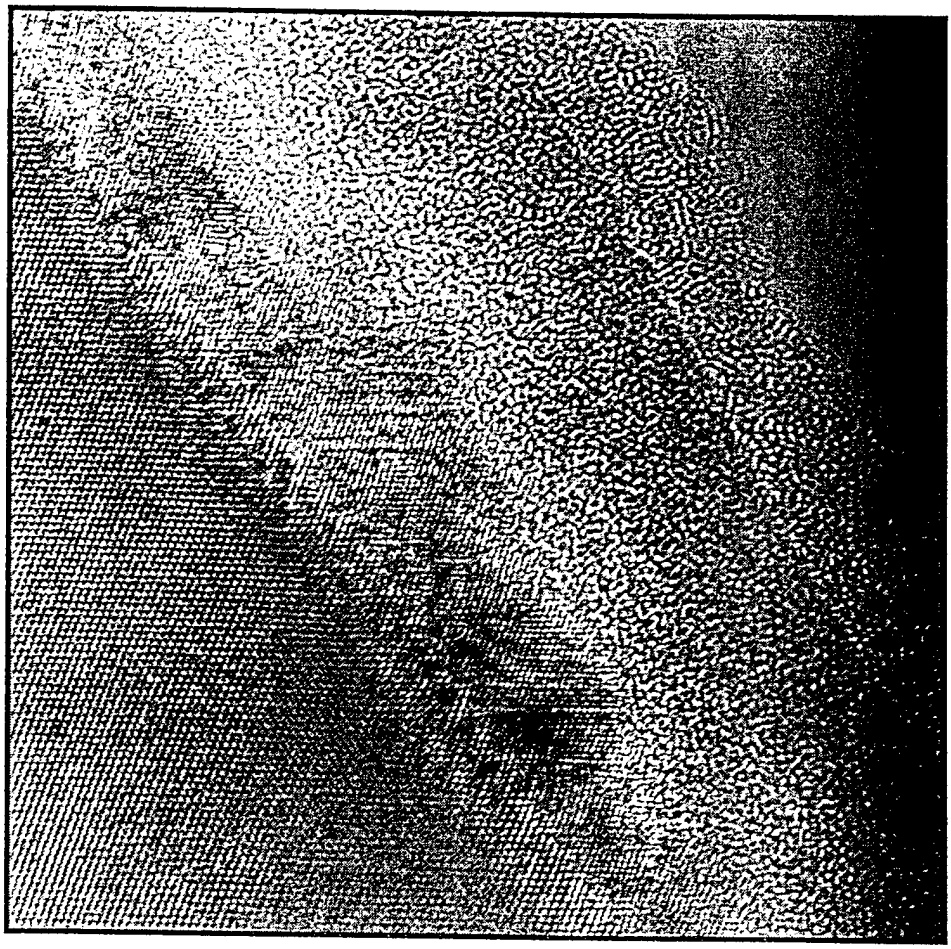


Figure 3. TEM of conversion.

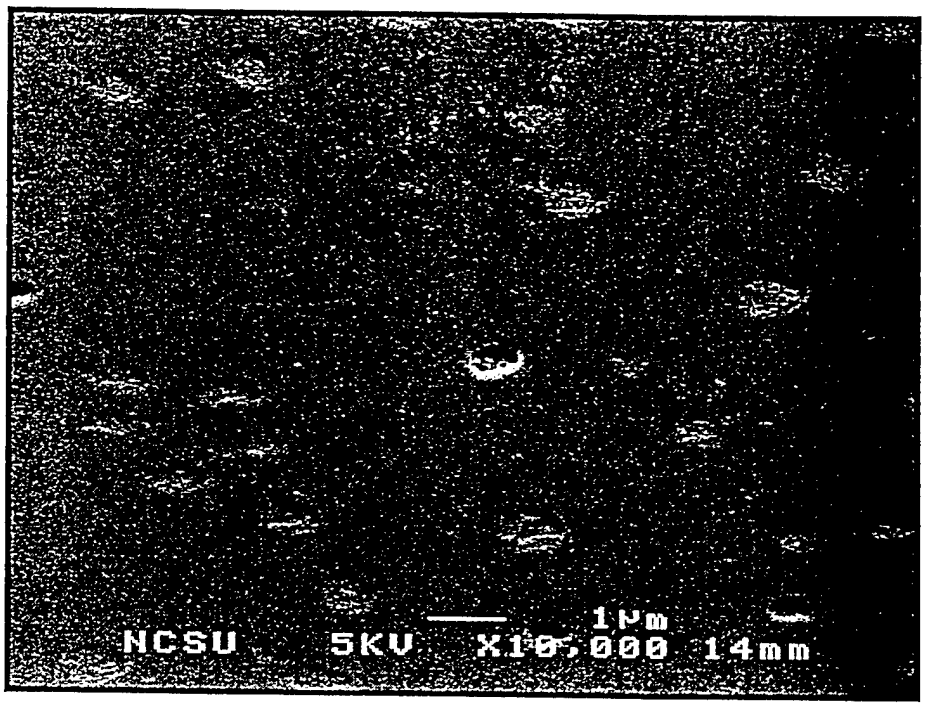
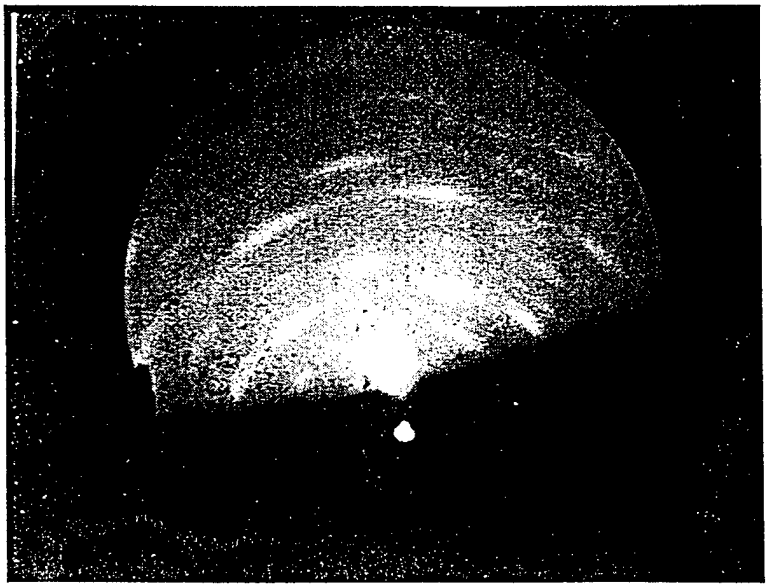


Figure 4. SEM of conversion on SIMOX.



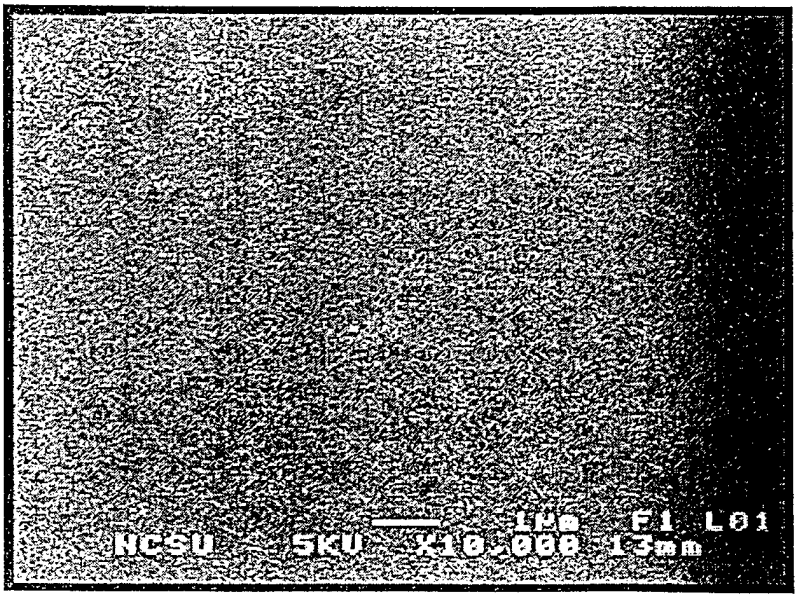


Figure 5. SEM and RHEED of AlN on Si(111).

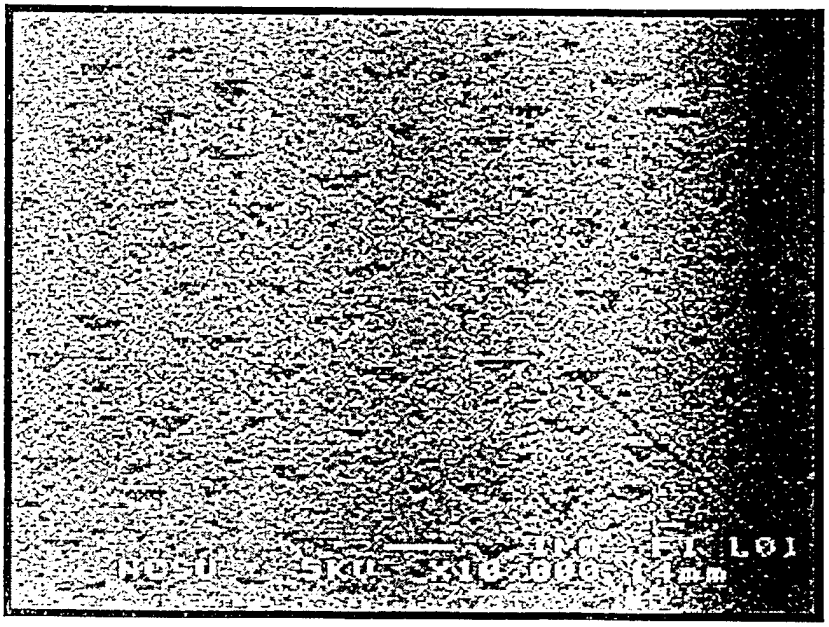


Figure 6. SEM and RHEED of AlN on converted SiC.

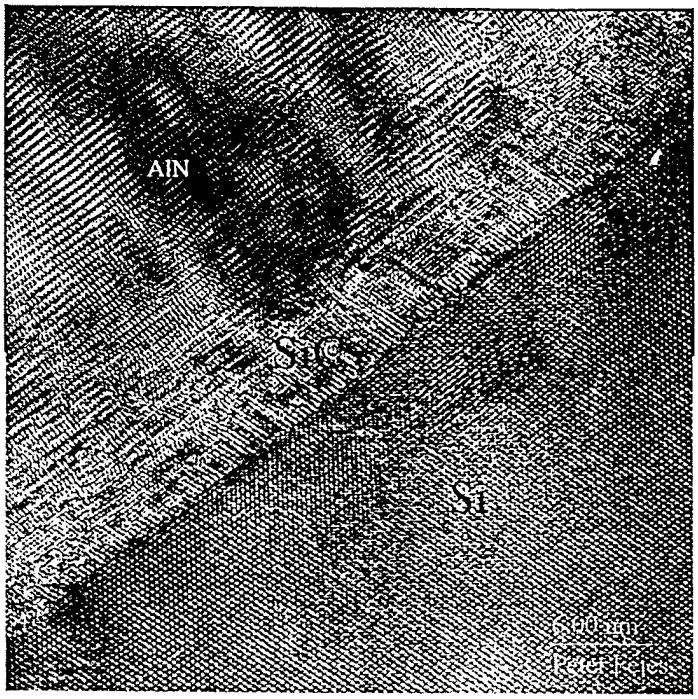


Figure 7. TEM of interfaces (substrate/SiC/AlN).

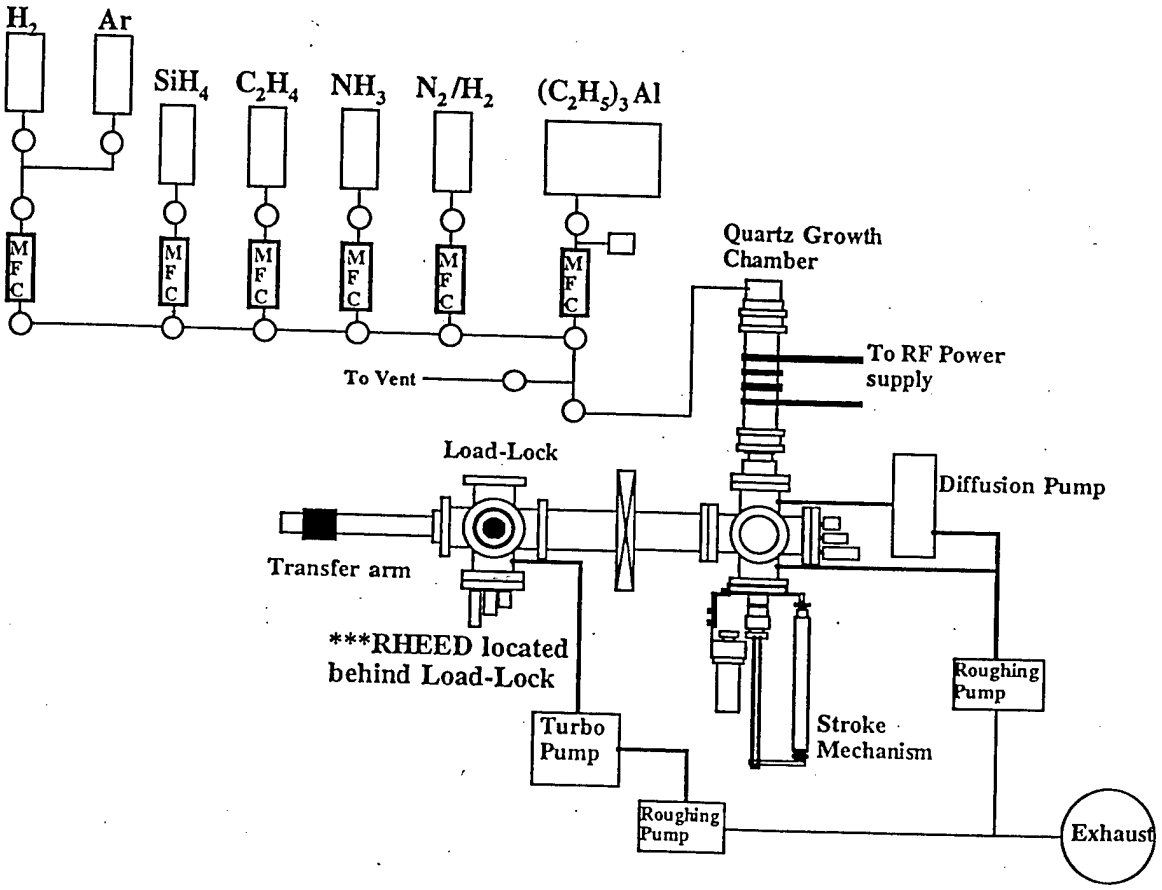


Figure 8. CVD system schematic.